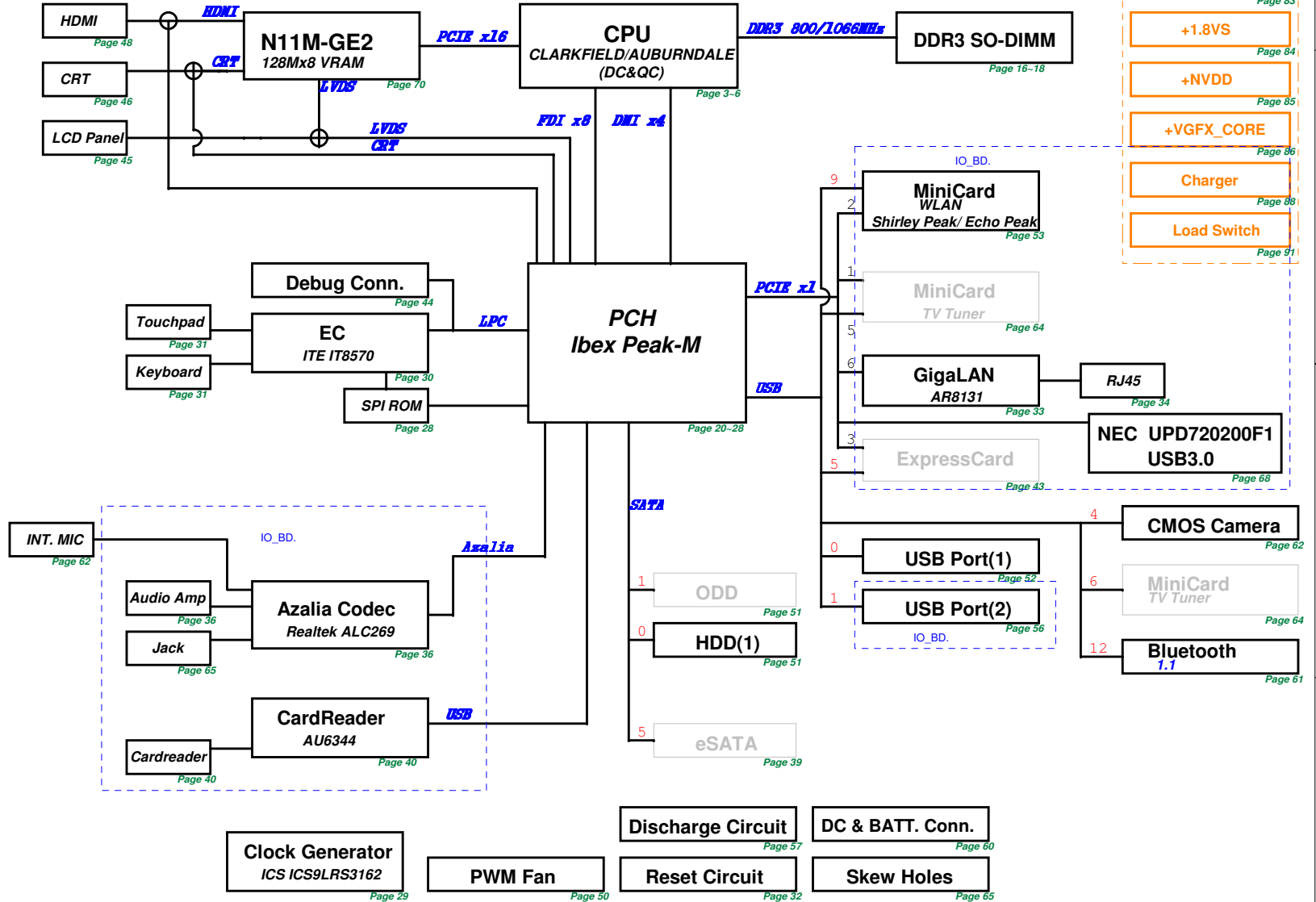


U35JC SCHEMATIC Revision 1.0

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81	PW_SYSTEM
82	PW_I/O_VTT_PCH
83	PW_I/O_DDR& VTT
84	PW_I/O_+1.8VS
85	PW_I/O_+NVDD
86	PW_+VGFX_CORE
88	PW_CHARGER
91	PW_LOAD SWITCH
93	PW_SIGNAL
94	PW_FLOWCHART

BLOCK DIAGRAM



PCH_IBEX
GPIO

PCH_IBEX GPIO	Use As	Signal Name	Internal & External Pull-up/down	Power
GPIO 00	Native	GPIO0	EXT PU	+3VS
GPIO 01	Native	GPIO1	INT PU, EXT PU	+3VS
GPIO [2:5]	Native	PCI_INT[E:H]#	EXT PU	+3VS
GPIO 06	GPI	DGPU_HPD_INTR#_R	INT PU, EXT PU	+3VS
GPIO 07	GPI	USB3_SMI#	INT PU, EXT PU	+3VS
GPIO 08	GPI	EXT_SMI#	EXT PU & INT PU	+3VSUS
GPIO 09	Native	-	EXT PU	+3VSUS
GPIO 10	Native	-	EXT PU	+3VSUS
GPIO 11	GPI	EXT_SCI#	EXT PU	+3VSUS_ORG
GPIO 12	Native	-	-	-
GPIO 13	Native	HDA_DOCK_RST#	INT PD	-
GPIO 14	Native	-	-	+3VSUS
GPIO 15	GPO	BT_LED	INT PD	-
GPIO 16	GPO	DGPU_HOLD_RST#	-	-
GPIO 17	GPI	DGPU_PWROK	EXT PD & INT PU	GND
GPIO 18	Native	CLK_REQ1_TV#	EXT PU	+3VS
GPIO 19	Native	SATA1GP	EXT PU	+3VS
GPIO 20	Native	CLKREQ2#_WLAN	EXT PD	GND
GPIO 21	Native	SATA0GP	EXT PU	+3VS
GPIO 22	GPO	WLAN_LED	-	-
GPIO 23	Native	LPC_DRQ#1	INT PU	-
GPIO 24	GPO	USB20_SEL	-	-
GPIO 25	Native	CLKREQ3_NEWCARD#	EXT PU	+3VSUS_ORG
GPIO 26	GPI	CLKREQ4_USB	EXT PD	GND
GPIO 27	Native	VRM_EN	INT PU	-
GPIO 28	GPO	WLAN_ON#	INT PU	-
GPIO 29	Native	ME_PM_SLP_LAN#_PCH	-	-
GPIO 30	GPO	ME_SusPwrDnAck	EXT PU	+3VSUS_ORG
GPIO 31	GPI	ME_AC_PRESENT_PCH	EXT PU	+3VSUS_ORG
GPIO 32	GPI	PM_CLKRUN#	EXT PU	+3VS
GPIO 33	GPI	HDA_DOCK_EN#	EXT PD, INT PU	GND
GPIO 34	Native	GPIO34	EXT PU	-
GPIO 35	Native	SATA_CLK_REQ#	EXT PD	-
GPIO 36	GPO	dGPU_PWR_EN#_GPIO36	-	-
GPIO 37	GPI	DGPU_PRSENT#	-	-
GPIO 38	GPI	PCB_ID0	EXT PD	-
GPIO 39	GPI	PCB_ID1	EXT PD	-
GPIO 40	Native	-	EXT PU	+3VSUS
GPIO 41	Native	-	EXT PU	+3VSUS
GPIO 42	Native	-	EXT PU	+3VSUS
GPIO 43	Native	-	EXT PU	+3VSUS
GPIO 44	Native	CLK_REQ5#	EXT PU	+3VSUS_ORG
GPIO 45	Native	CLK_REQ6#	EXT PD, INT PU	+3VSUS_ORG
GPIO 46	Native	CLK_REQ7#	EXT PU	+3VSUS_ORG
GPIO 47	Native	CLKREQ_PEG#_R	EXT PU/PD	+3VSUS_ORG
GPIO 48	Native	GPIO48	EXT PU	+3VS
GPIO 49	GPO	PCH_TEMP_ALERT#	EXT PU	+3VS
GPIO 50	Native	PCI_REQ1#	EXT PU	+3VS
GPIO 51	Native	PCI_GNT1#	INT PU	-
GPIO 52	GPO	dGPU_SELECT#_GPIO52	-	+3VS
GPIO 53	Native	-	INT PU	-
GPIO 54	Native	PCI_REQ3#	EXT PU	+3VS
GPIO 55	Native	PCI_GNT3#	EXT PU, INT PU	+3VS
GPIO 56	Native	CLKREQ_GLAN#	EXT PD	GND
GPIO 57	GPO	BT_ON	-	-
GPIO 58	GPI	SML1_CLK	EXT PU	+3VSUS_ORG
GPIO 59	Native	-	EXT PU (Not used)	+3VSUS
GPIO 60	Native	SML0ALERT#	EXT PU	+3VSUS_ORG
GPIO 61	Native	PM_SUS_STAT#	-	-
GPIO 62	Native	SUS_CLK	-	-
GPIO 63	Native	SLP_S5#	-	-
GPIO 64	Native	CLK_OUT0	INT PD	-
GPIO 65	Native	CLK_OUT1	INT PD	-
GPIO 66	GPO	CLK_OUT2	INT PD	-
GPIO 67	GPO	CLK_OUT3	-	-
GPIO 72	Native	PW_BATLOW#	EXT PU, INT PU	+3VSUS_ORG
GPIO 73	Native	CLK_REQ0#	INT PU	+3VSUS_ORG
GPIO 74	Native	SML1ALERT#	EXT PU	+3VSUS_ORG
GPIO 75	GPI	SML1_DAT	EXT PU	+3VSUS_ORG

EC GPIO	Use As	Signal Name
GPA0	0	PWR_LED#
GPA1	0	CHG_LED#
GPA2	0	CHG_FULL_LED#
GPA3	-	-
GPA4	0	LCD_BL_PWM
GPA5	0	FAN_PWM
GPA6	-	-
GPA7	-	-
GPB0	0	BATSEL_0
GPB1	0	BATSEL_1
GPB2	-	ME_AC_PRESENT_EC
GPB3	IO	SMB0_CLK
GPB4	IO	SMB0_DAT
GPB5	0	A20GATE
GPB6	0	RCIN#
GPB7	0	PM_RSMRST#
GPC0	0	Clock_select_uc
GPC1	IO	SMB1_CLK
GPC2	IO	SMB1_DAT
GPC3	0	PM_PWRBTN#
GPC4	I	AC_IN_OC#
GPC5	0	OP_SD#
GPC6	I	BAT1_IN_OC#
GPC7	I	RFON_SW#
GPD0	I	PWRLIMIT#
GPD1	I	PM_SUSC#
GPD2	I	BUF_PLT_RST#
GPD3	0	EXT_SCI#
GPD4	0	EXT_SMI#
GPD5	0	LCD_BACKOFF#
GPD6	I	FAN0_TACH
GPD7	I	HDMI_HP_EC
GPE0	-	-
GPE1	-	-
GPE2	-	-
GPE3	-	-
GPE4	I	PWR_SW#
GPE5	-	-
GPE6	I	LID_SW#
GPE7	I	MARATHON#
GPFO	0	-
GPFI	0	VSUS_ON
GPFF2	0	VCCP_DV0
GPFF3	0	VCCP_DV1
GPFF4	I	TP_CLK
GPFF5	IO	TP_DAT
GPFF6	0	THRO_CPU
GPFF7	I	PCH_SPI_OV
GPFG0	I	ME_SusPwrDnAck_EC
GPFI1	I	PM_SUSB#
GPFG2	-	-
GPFG6	-	-
GPFI0	IO	PM_CLKRUN#
GPFI1	0	GFV_VR_ON
GPFI2	0	CHG_EN
GPFI3	0	SUSC_EC#
GPFI4	0	SUSB_EC#
GPFI5	0	NUM_LED#
GPFI6	0	CAP_LED#
GPFI0	I	VGA_ALERT#
GPFI1	I	SUS_PWRGD
GPFI2	I	ALL_SYSTEM_PWRGD
GPFI3	I	VRM_PWRGD
GPFI4	I	PCH_TEMP_ALERT#
GPFI5	I	CPU_ISENSE
GPFI6	I	GPU_ISENSE
GPFI7	I	VCORE_CMSET
GPJ0	0	CPU_VRON
GPJ1	0	PM_PWROK
GPJ2	0	VSET_EC
GPJ3	0	ISET_EC
GPJ4	0	CPU_DV0
GPJ5	0	CPU_DV1

EC
IT8570

PCIE 1	
PCIE 2	Minicard WLAN
PCIE 3	
PCIE 4	USB 3.0
PCIE 5	
PCIE 6	GLAN
PCIE 7	
PCIE 8	

SATA 0	SATA HDD (1)
SATA1	
SATA4	
SATA5	

USB 0	USB Port (1)
USB 1	Card Reader(2.0)
USB 2	USB Port (3)
USB 3	
USB 4	
USB 5	
USB 6	
USB 7	
USB 8	WiFi/WiMax
USB 9	Camera
USB 10	
USB 11	
USB 12	Bluetooth
USB 13	

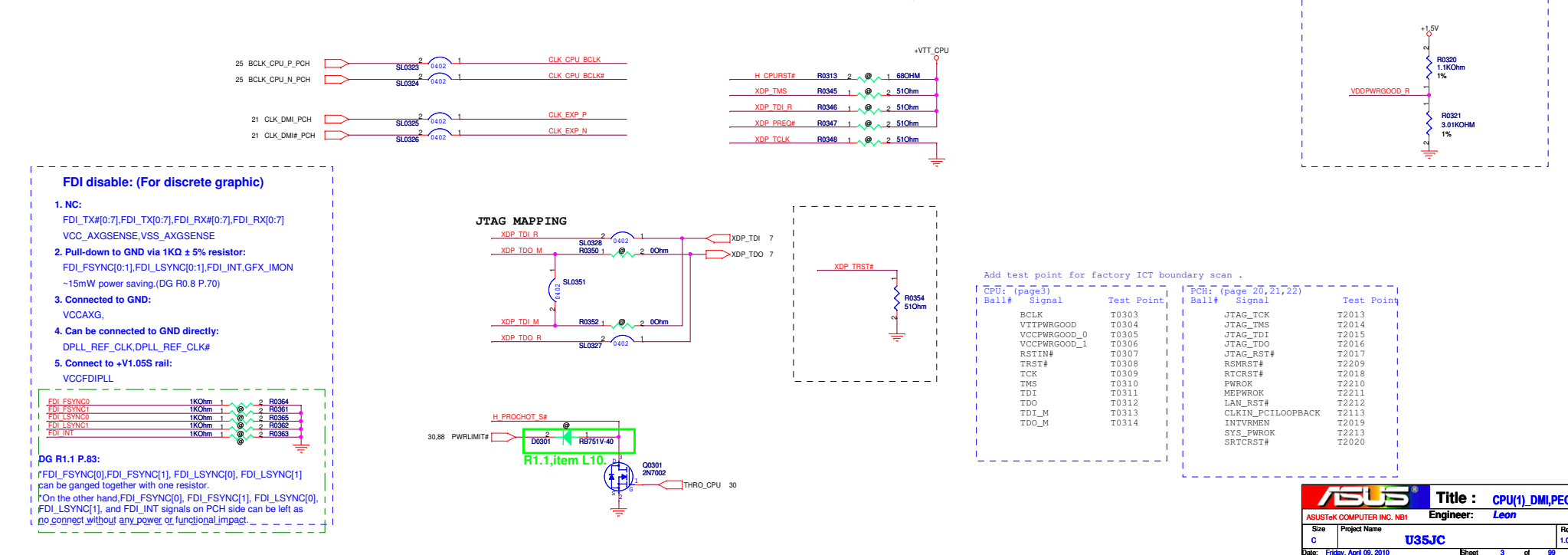
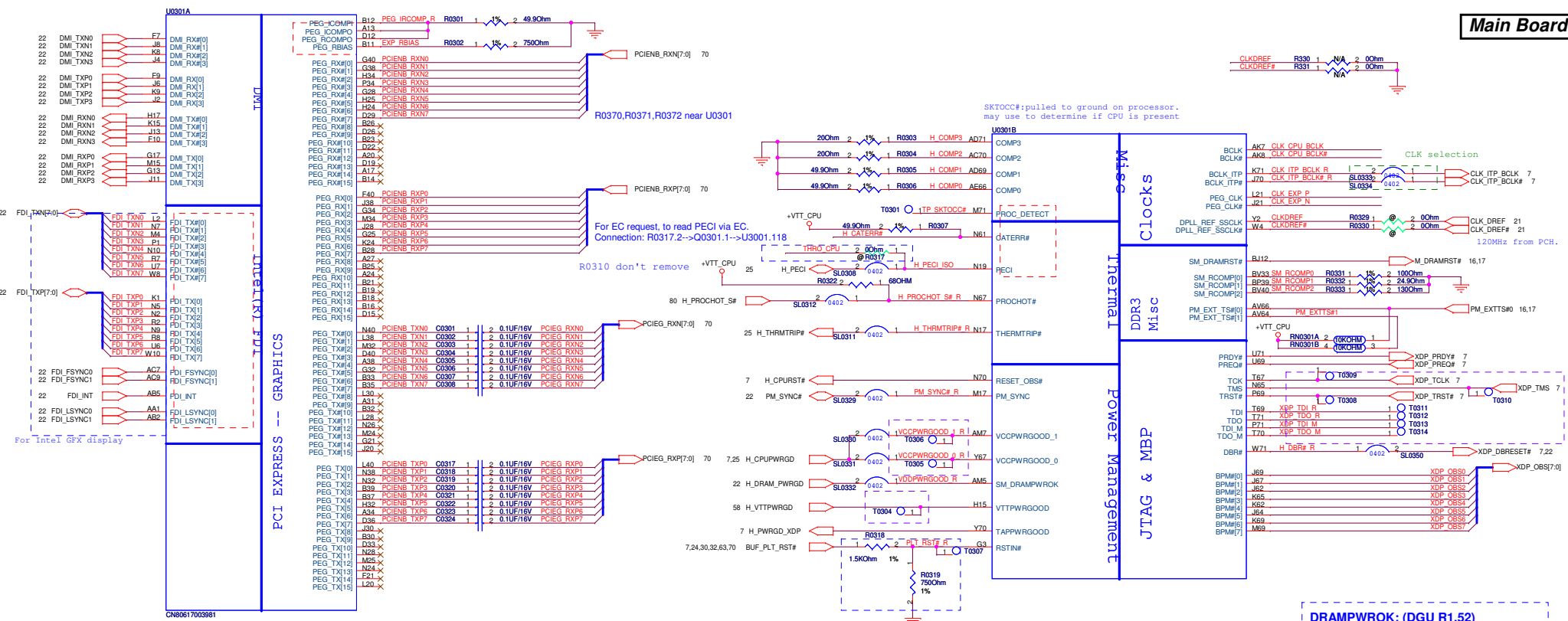
SM_BUS ADDRESS :

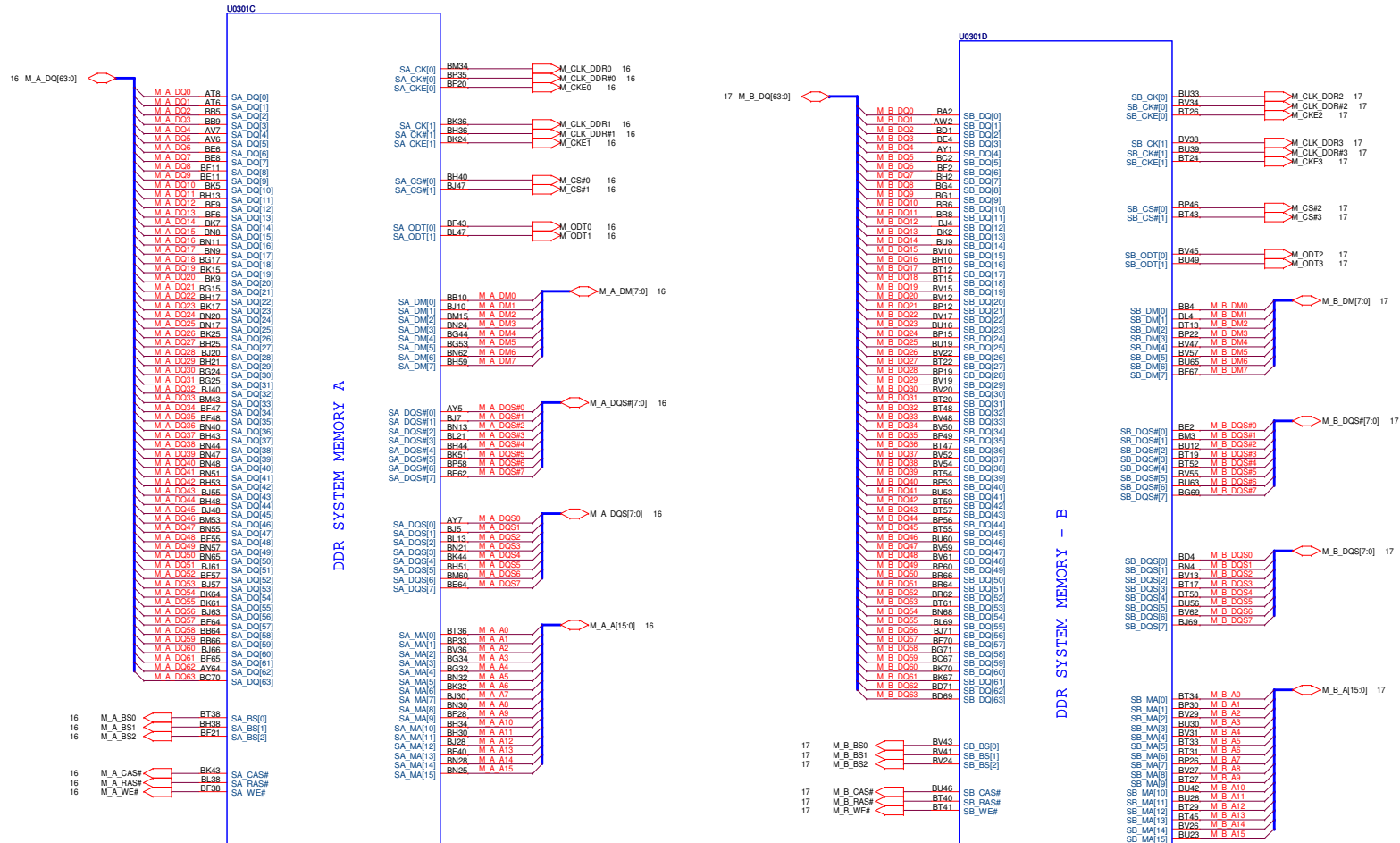
PCH Master		
SM-Bus Device	SM-Bus Address	
Clock Generator(ICS9LV3162BKLFT)	1101001x (D2)	
SO-DIMM 0	1010000x (A0)	
SO-DIMM 1	1010001x (A2)	
WiFi/WiMax	N/A	
EC Master (SMB1)		
SM-Bus Device	SM-Bus Address	
INA219AIDCNR(CPU)	x1000000 (40)	
INA219AIDCNR(VGA)	x1000001 (41)	

Device Identification

	CPU Thermal Sensor P/N:	component name
1st	06G073050010	Current/Power Monitor
S		
S		

	Clock Gen P/N:	component name
1st	06G011604010	ICS9LR53197
S		
S		





CN80617003981

CN80617003981

CFG strapping information:

CFG[1:0]: PCI Express Port Bifurcation:(Clarksfield Only)

- 11 = 1 x 16 PEG (Default)
- 10 = 2 x 8 PEG

CFG[3]: PCIE Static Numbering Lane Reversal.(Auburndale Only)

- 1: Normal Operation (Default)
- 0: Lane Numbers Reversed 15 -> 0, 14 -> 1, ...

CFG[4]: Embedded DisplayPort Detection.(Auburndale Only)
 1: Disabled - No Physical Display Port attached to Embedded DisplayPort

- 1:Disabled - No Physical Display Port attached to Embedded DisplayPort
- 0:Enabled - An external Display Port device is connected to the Embedded Display Port

CFG[7]: Fixed for PCI Express 2.0 jitter specifications. (Clarksfield)

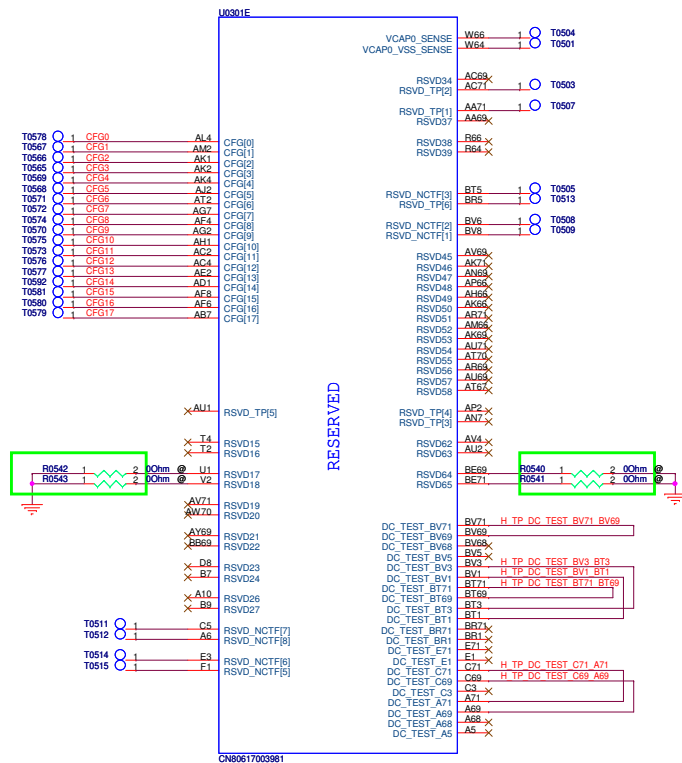
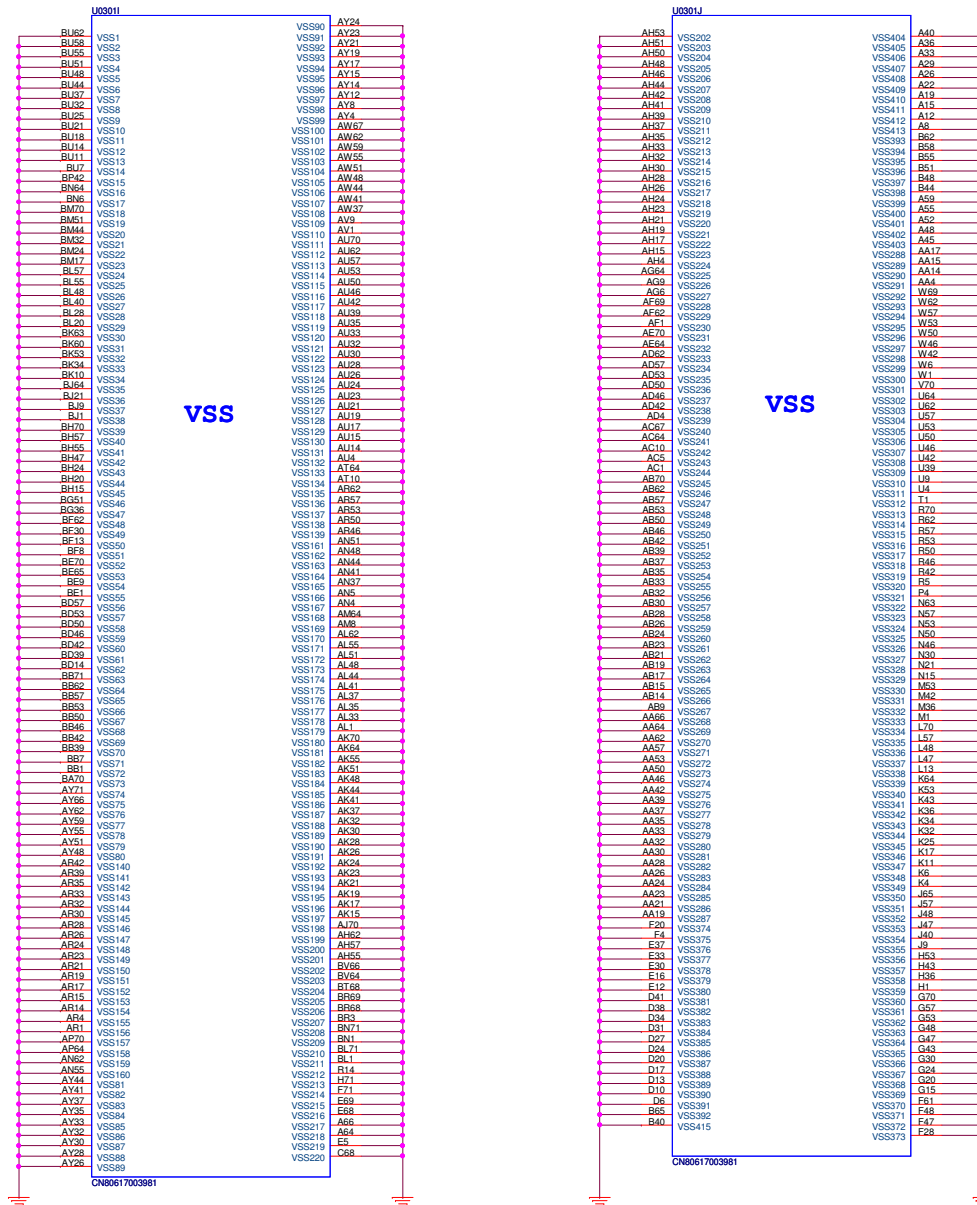
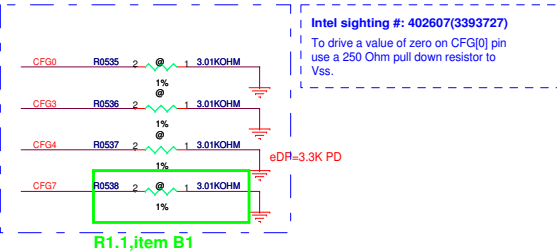
Clarksfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm/5% resistor
For a common motherboard design (for AUB and CFD),

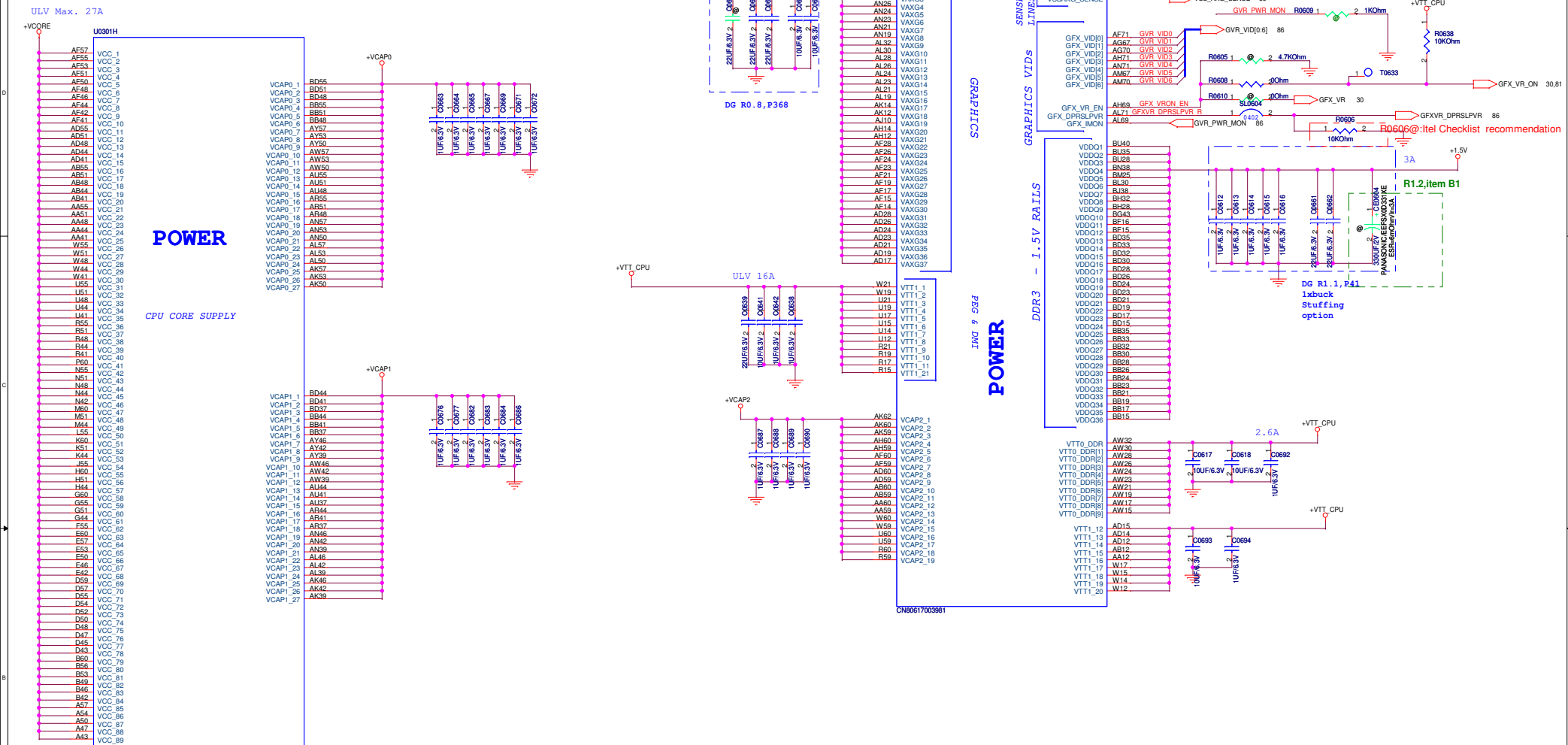
For a common motherboard design (for AUB and GUB), the pull-down resistor should be used. Does not impact AUB functionality.

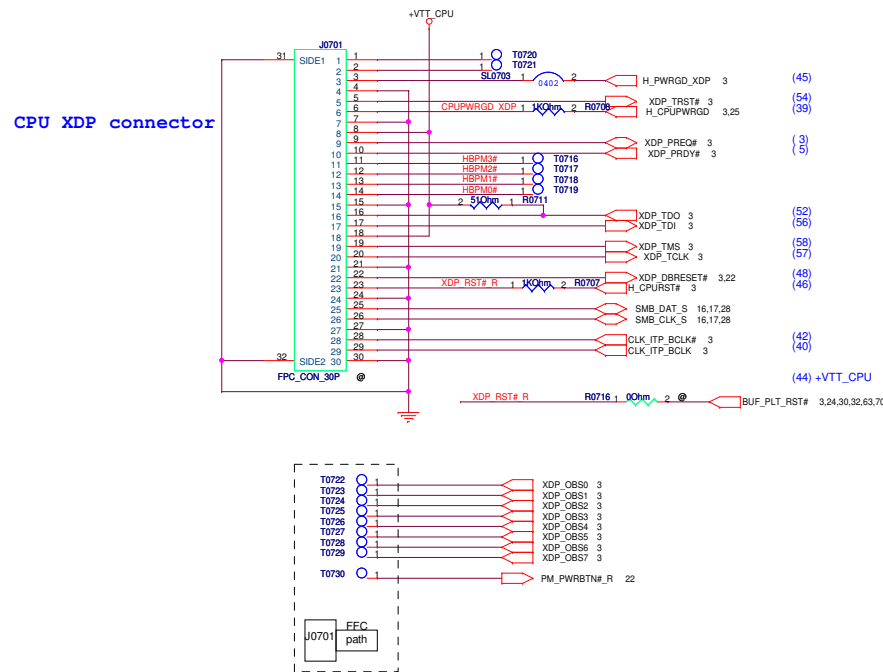
Unmount if Intel has fixed this issue.

Note: (Auburndale) Hardware Straps are sampled on the asserting edge of VCCPWRGOOD_0 and VCCPWRGOOD_1 and latched inside the processor.

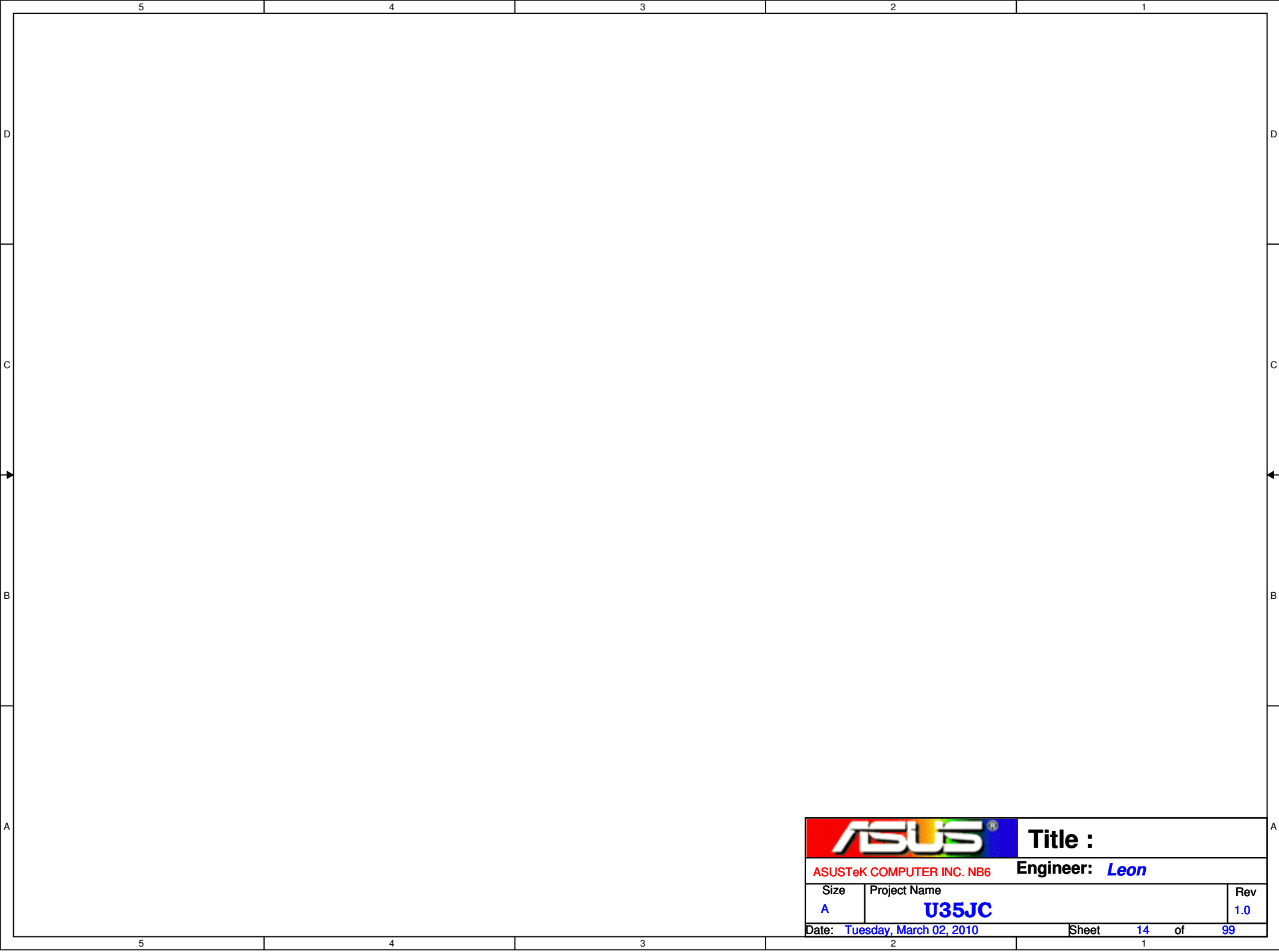
Note: (Clarksfield)Hardware Straps are sampled after RSTIN# de-assertion.












		Title :	
ASUSTeK COMPUTER INC. NB6		Engineer: Leon	
Size	Project Name		Rev
A	U35JC		1.0
Date: Tuesday, March 02, 2010		Sheet	14 of 99

D

C

B

A



Title :

ASUSTeK COMPUTER INC. NB6

Engineer: *Leon*

Size

A

Project Name

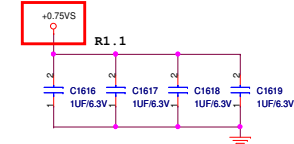
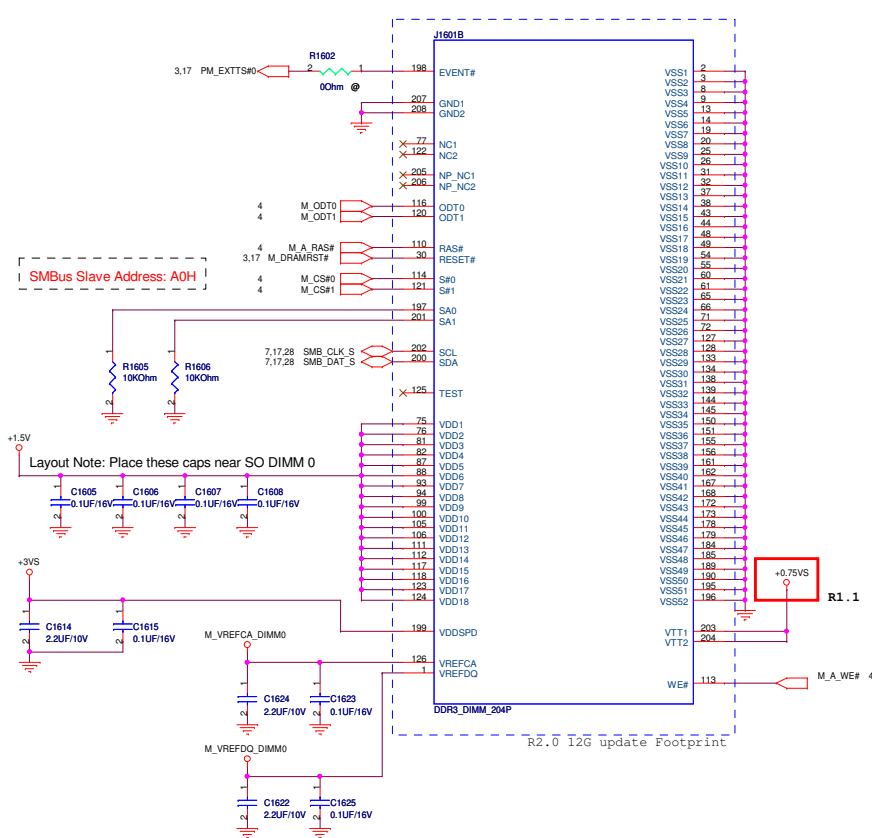
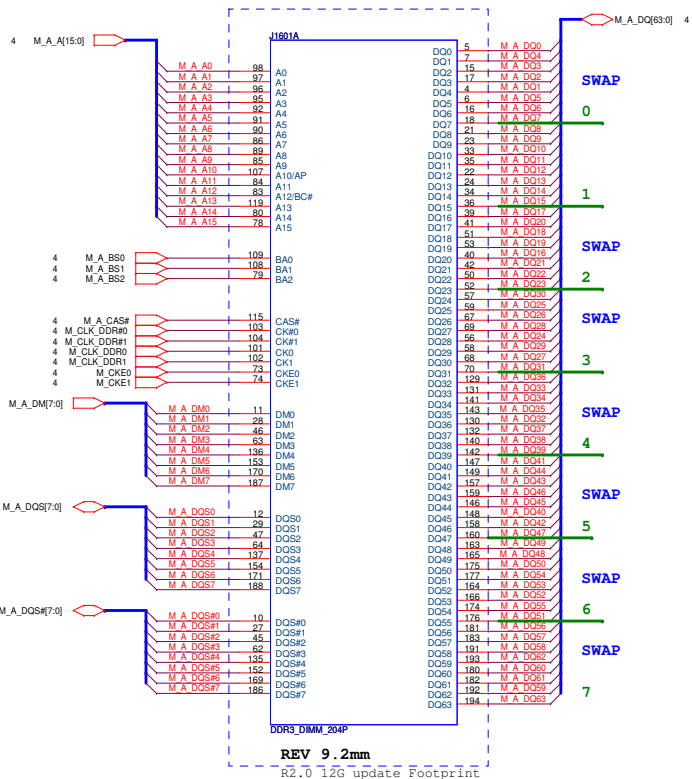
U35JC

Rev

1.0

Date: Tuesday, March 02, 2010

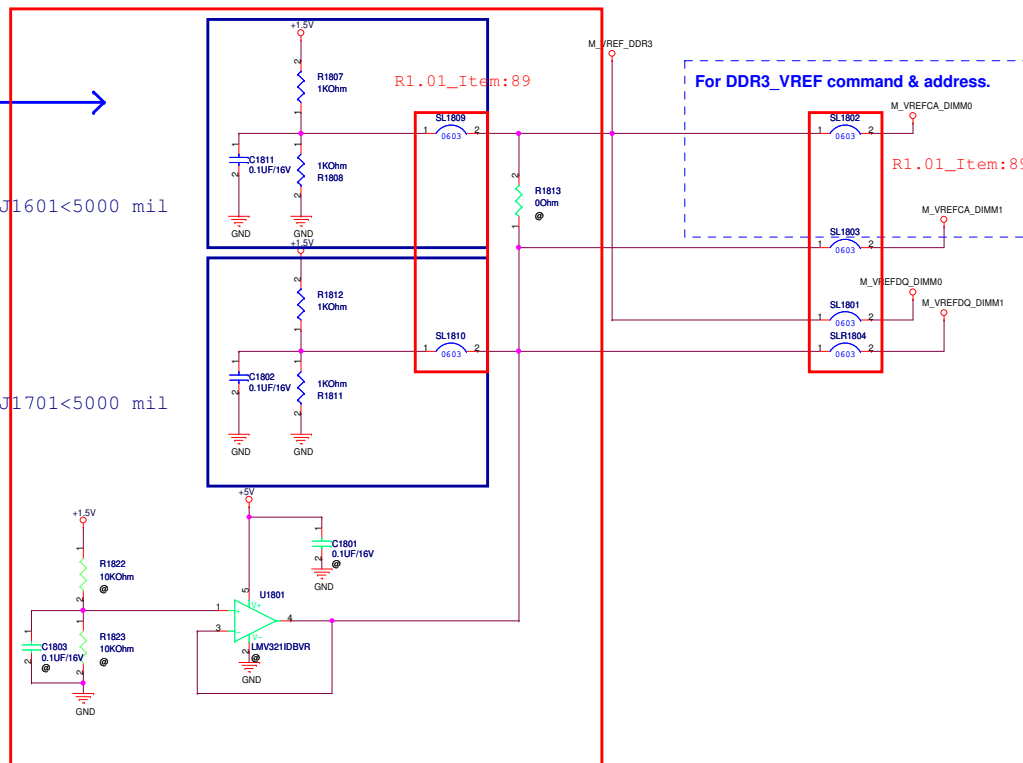
Sheet 15 of 99

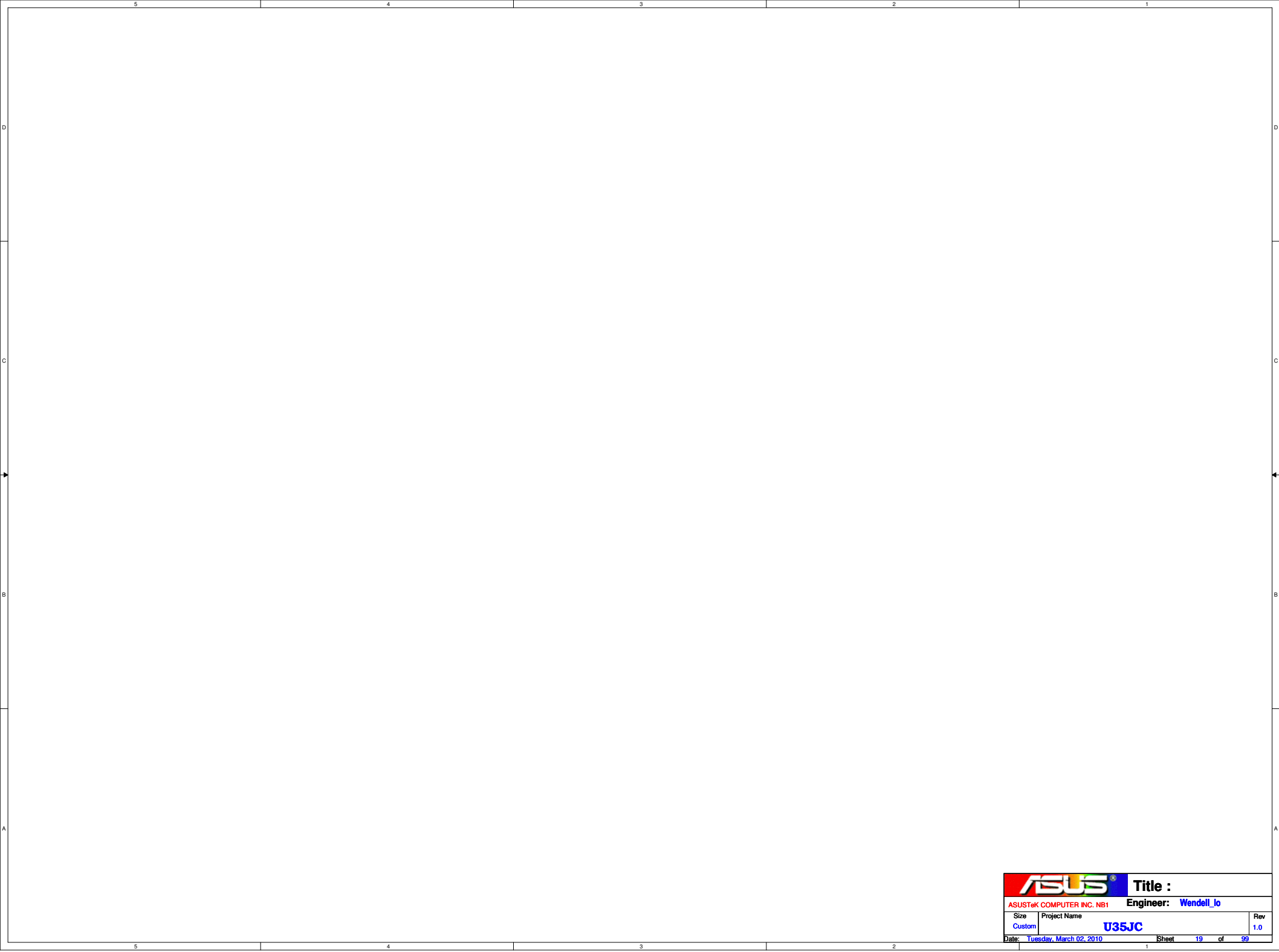



Default M1 →

Near J1601<5000 mil

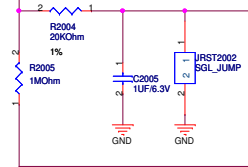
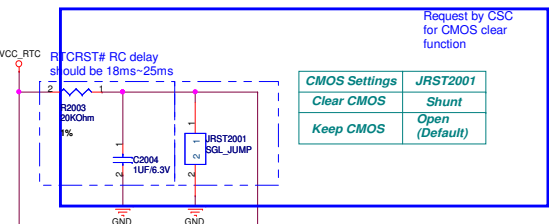
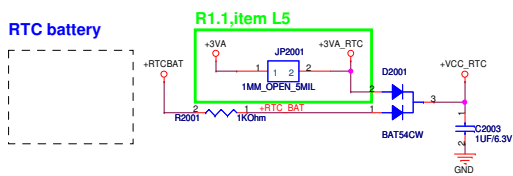
Near J1701<5000 mil



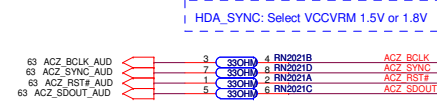


		Title :	
ASUSTeK COMPUTER INC. NB1		Engineer: Wendell_lo	
Size	Project Name		Rev
Custom	U35JC		1.0
Date: Tuesday, March 02, 2010		Sheet	19 of 99

RTC battery



TPM Settings	JRST2002
Clear ME RTC Registers	Shunt
Keep ME RTC Registers	Open (Default)



414044 Design Guide R1.11 Update: page9

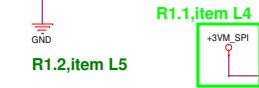
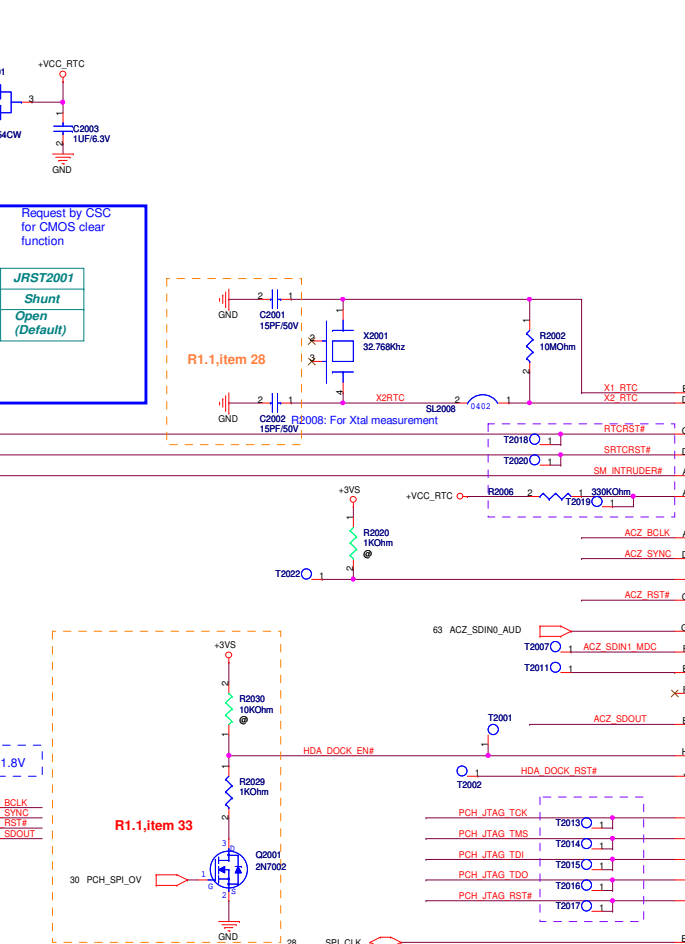
GPIO33:
This signal should be only asserted low through an external pull-down in manufacturing or debug environments ONLY.
Without connecting GPIO33, customers may not be able to override SPI flash contents.

Strap information:

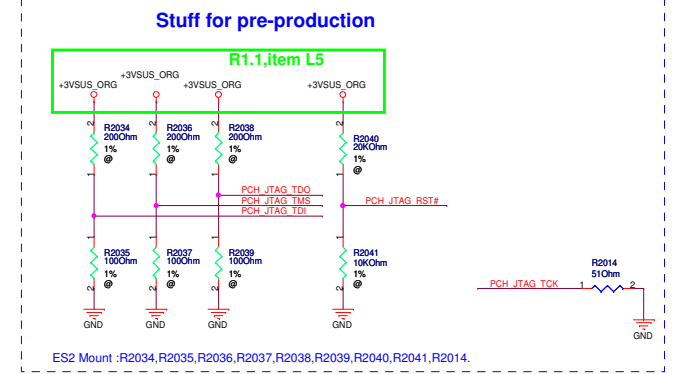
HDA_SPKR: No reboot strap
Low: Disable.
High: Enable

HDA_DOCK_EN#:
1. Flash descriptor security:
Sampled low: override
Sampled high: in effect.
2. GPIO33 low on the rising edge of PWROK,
Will also disable Intel ME.

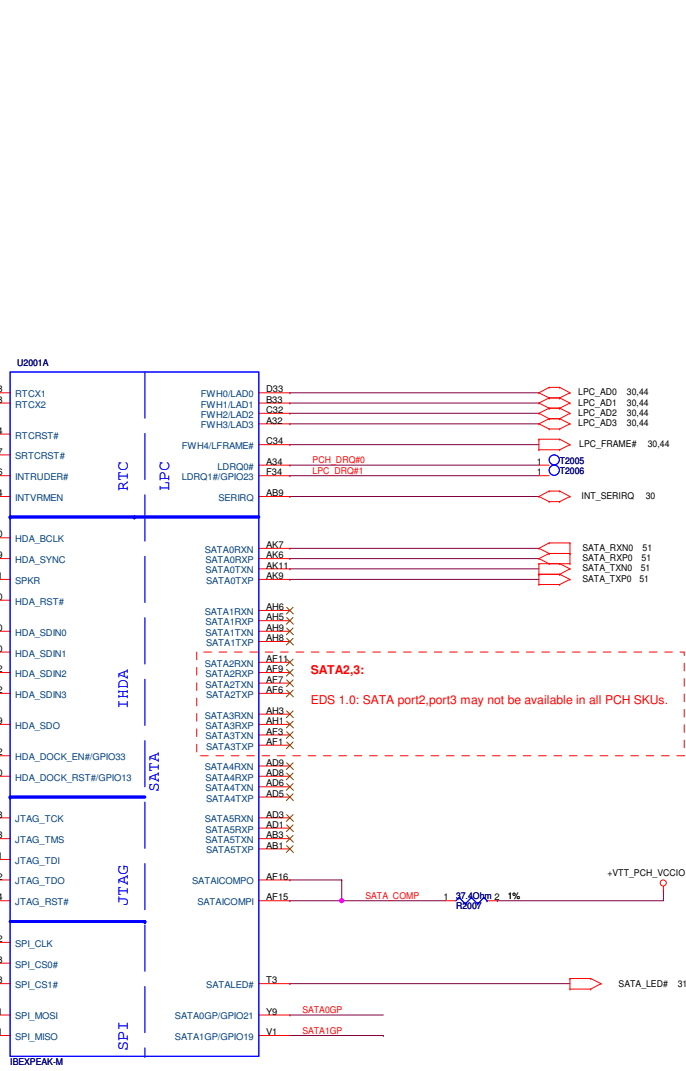
SPI_MOSI: ITPM strap.
Mount R2015: Enable
Unmount R2015: Disable(default)



MoW50 IbeXPeak JTAG requirements:

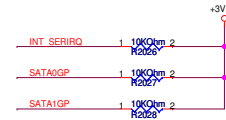


ES2 Mount :R2034,R2035,R2036,R2037,R2038,R2039,R2040,R2041,R2044.

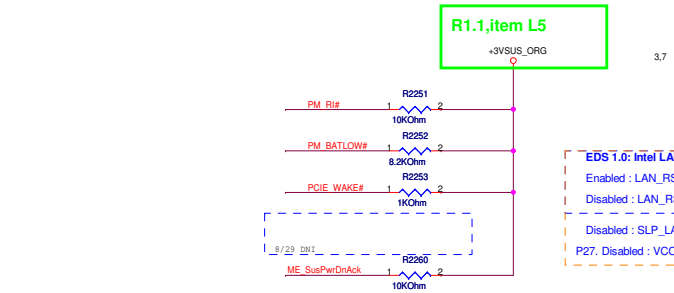
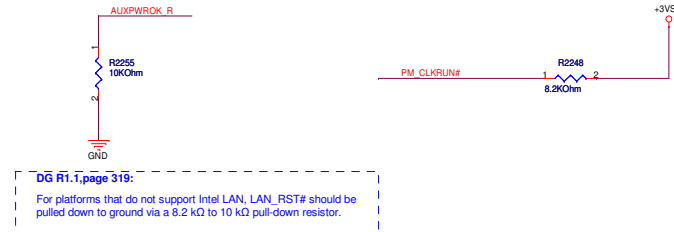


MoW36 IbeXPeak JTAG requirements:

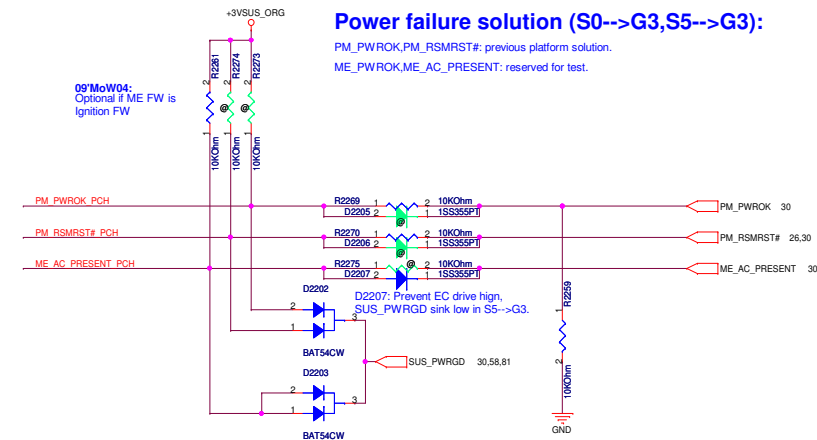
ES1 Enable:Mount R2034,R2035,R2036,R2037,R2040,R2041,R2044.
DNI R2038,R2039. (TDO)
ES1 Disable:Mount R2040,R2041,R2044.
DNI: others.

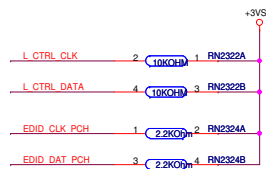


pre-ES1 not support
Reversal Feature



R1.1, item L15





LVDS Disable: (For discrete graphic)

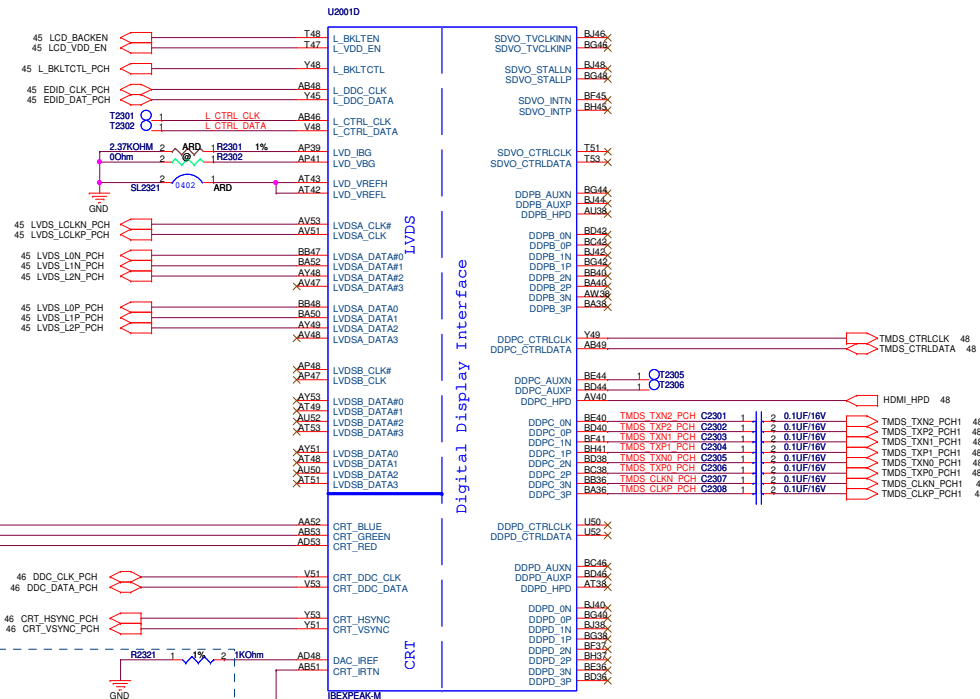
1. NC:
LVDSA_DATA [3:0], LVDSA_DATA# [3:0],
LVDSA_CLK, LVDSA_CLK#, LVDSB_DATA [3:0],
LVDSB_DATA# [3:0], LVDSB_CLK, LVDSB_CLK#
L_VDD_EN, L_BKLTEN, L_BKLTCTL, LVD_VREFH
LVD_VREFL, LVD_IBG, LVD_VBG
2. Connected to GND:
VccALVDS, VccTX_LVDS

46 CRT_B_PCH
46 CRT_G_PCH
46 CRT_R_PCH

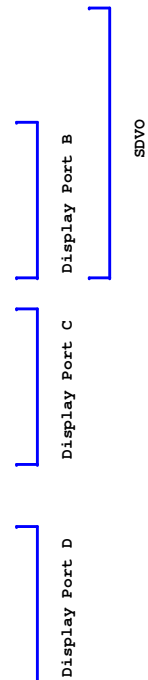
CRT Disable: (For discrete graphic)

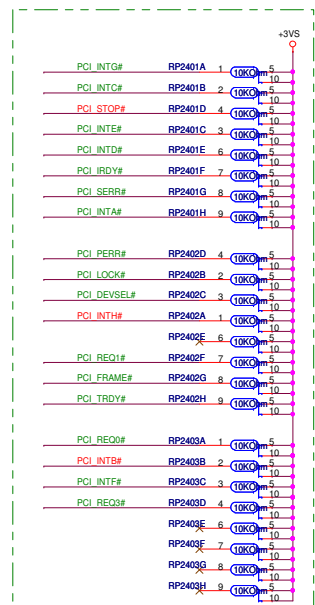
1. NC:
CRT_RED, CRT_GREEN, CRT_BLUE
CRT_HSYCN, CRT_VSYCN
2. 1-k Ω \pm 0.5% pull-down to GND:
DAC_IREF
3. Connected to GND:
CRT_ITRN
4. Connect to +V3.3:
VCCADAC

Design guide 1.62 updated: DAC_IREF CFD: 1Kohm/5% ; ARD: 1Kohm/0.5%
整合料件改為1%

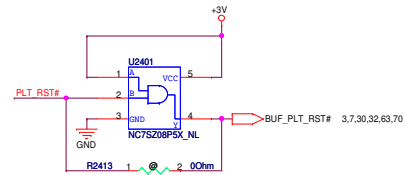


DDPB_HPD: V112 max=0.8V,
V1h2 min=2V



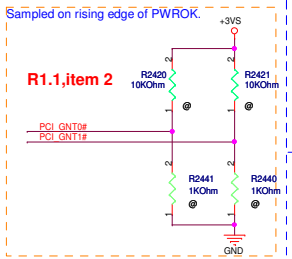


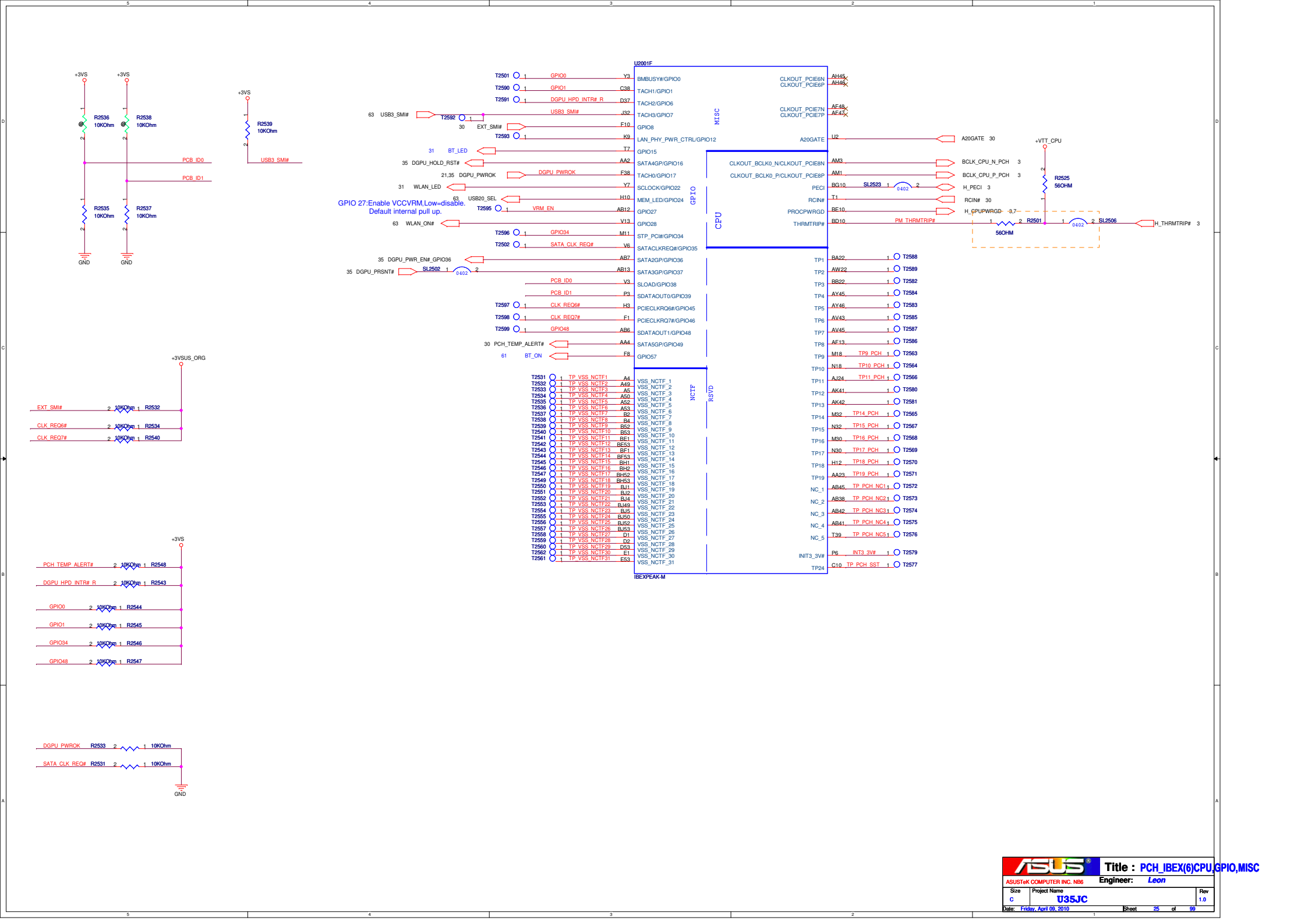
PCI_INTG#	RP2A01A	1	10KΩ	5
PCI_INTC#	RP2A01B	2	10KΩ	5
PCI_STOP#	RP2A01D	4	10KΩ	5
PCI_INTF#	RP2A01C	3	10KΩ	5
PCI_INTD#	RP2A01E	5	10KΩ	5
PCI_IRDY#	RP2A01F	6	10KΩ	5
PCI_SERR#	RP2A01G	8	10KΩ	5
PCI_INTA#	RP2A01H	9	10KΩ	5
PCI_PERR#	RP2A02D	4	10KΩ	5
PCI_LOCK#	RP2A02B	2	10KΩ	5
PCI_DEVSEL#	RP2A02C	3	10KΩ	5
PCI_INTM#	RP2A02A	1	10KΩ	5
	RP2A02E	6	10KΩ	5
PCI_REQ0#	RP2A02F	7	10KΩ	5
PCI_FRAME#	RP2A02G	8	10KΩ	5
PCI_TRDY#	RP2A02H	9	10KΩ	5
PCI_REQ0#	RP2A03A	1	10KΩ	5
PCI_INTB#	RP2A03B	2	10KΩ	5
PCI_INTF#	RP2A03C	3	10KΩ	5
PCI_REQ3#	RP2A03D	4	10KΩ	5
	RP2A03E	6	10KΩ	5
	RP2A03F	7	10KΩ	5
	RP2A03G	8	10KΩ	5
	RP2A03H	9	10KΩ	5

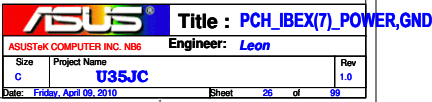


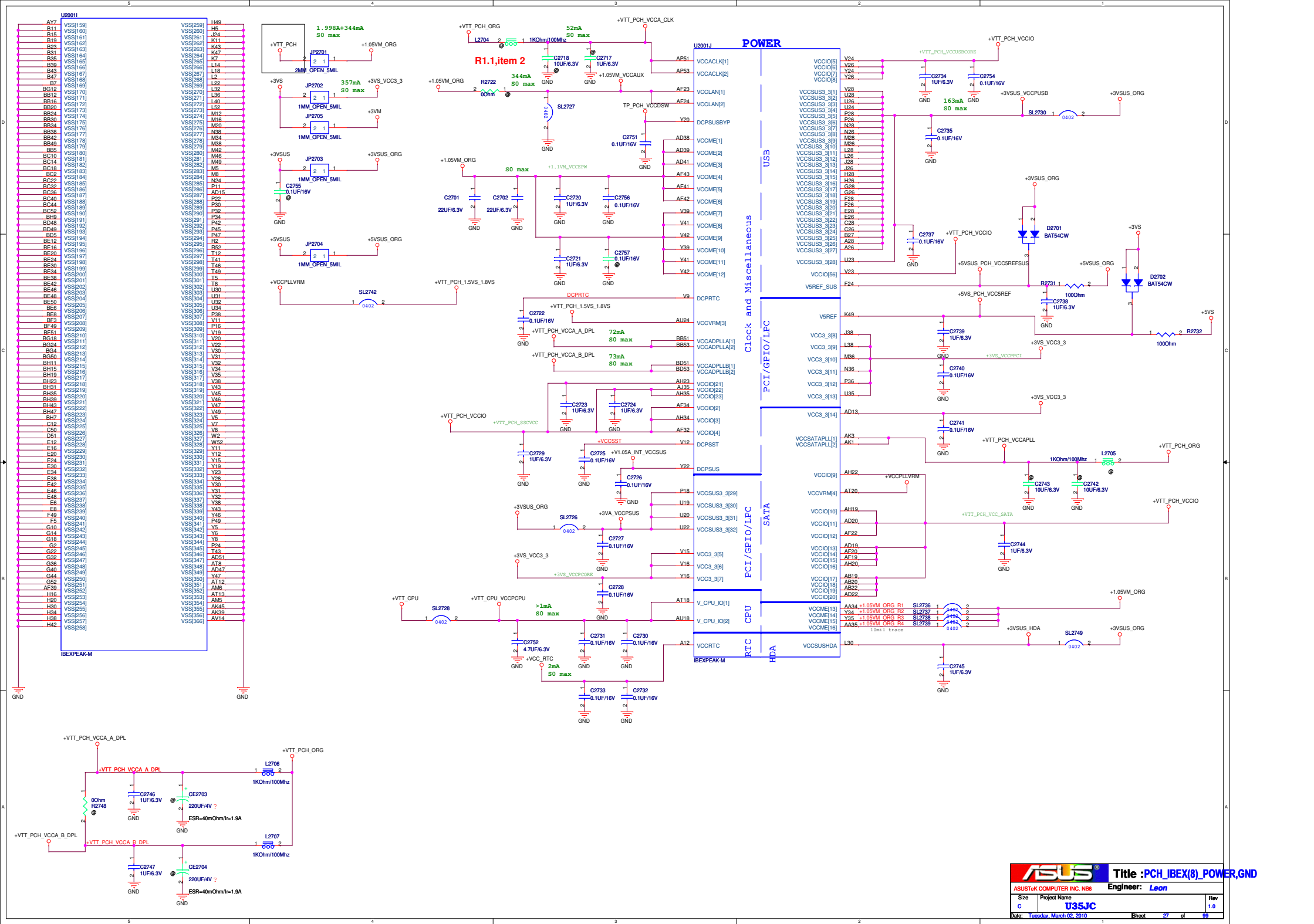
**GNT3#: A16 swap override Strap/
Top-Block swap override jumper**

Low=Enabled A16 swap override/ Top-Block swap override
High=Default

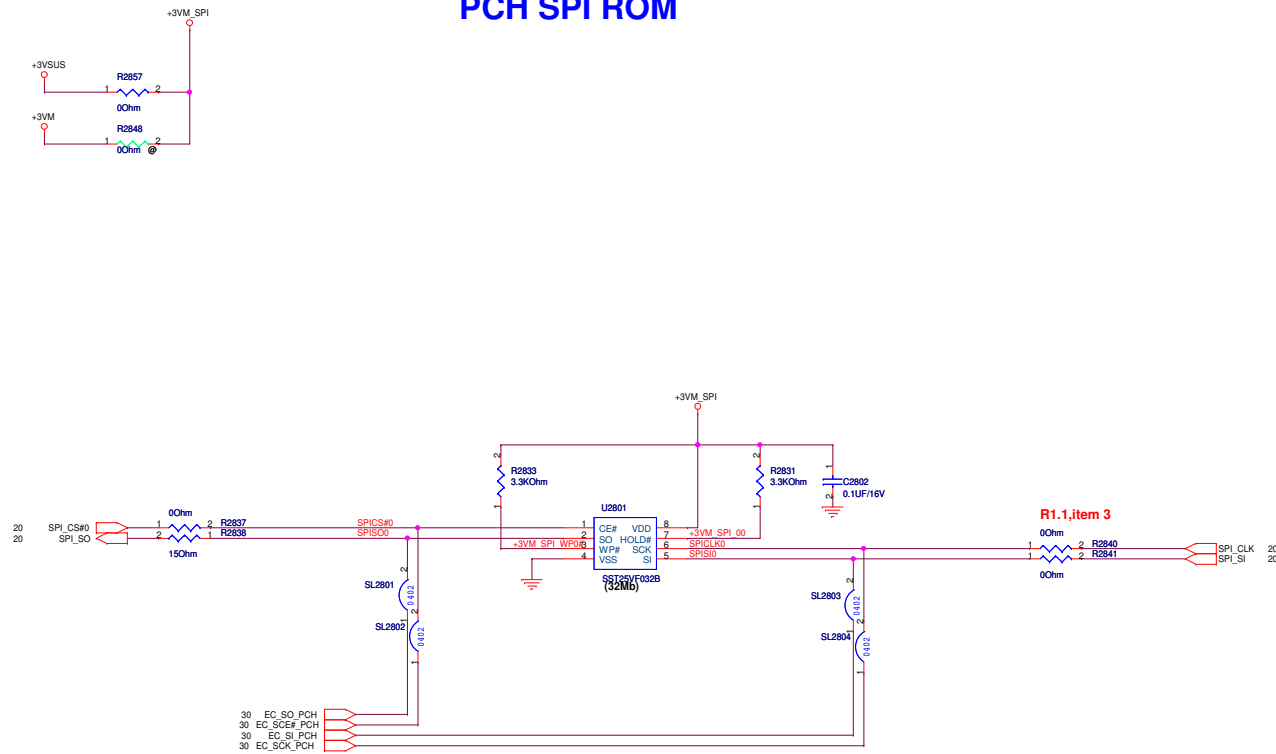




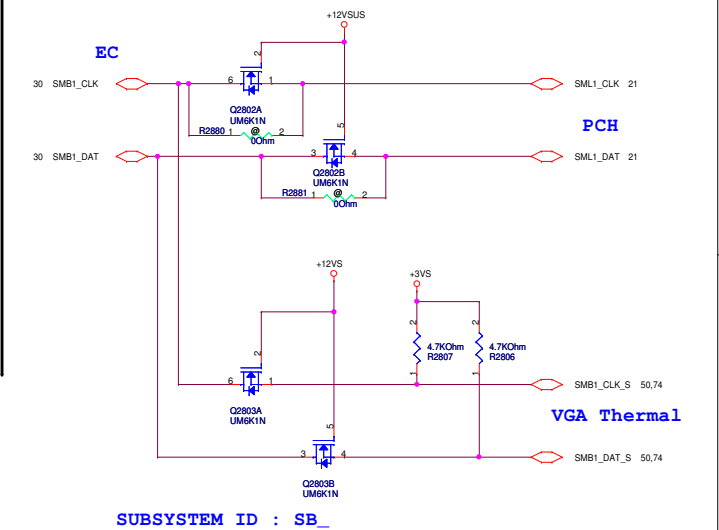
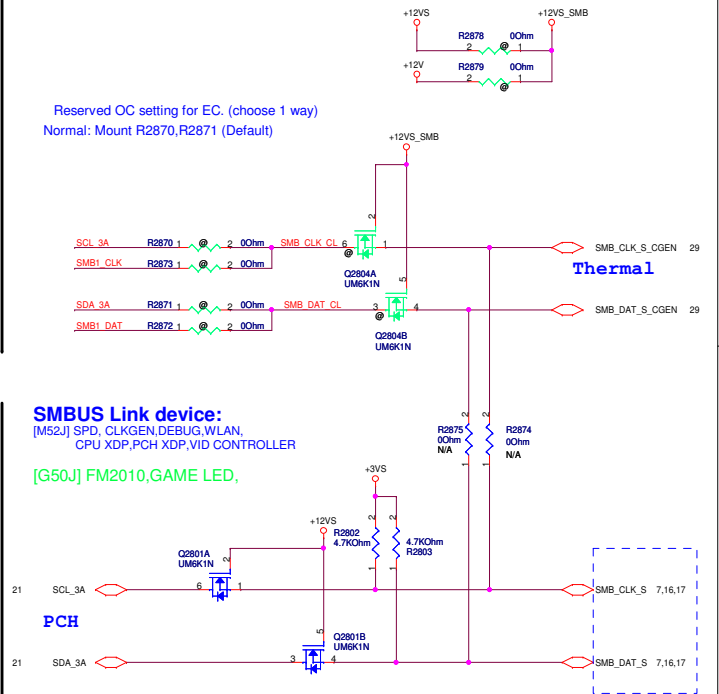





PCH SPI ROM



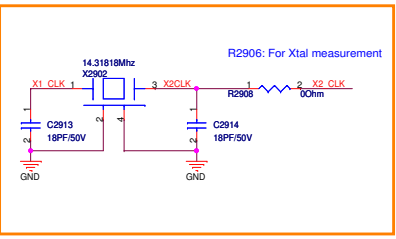
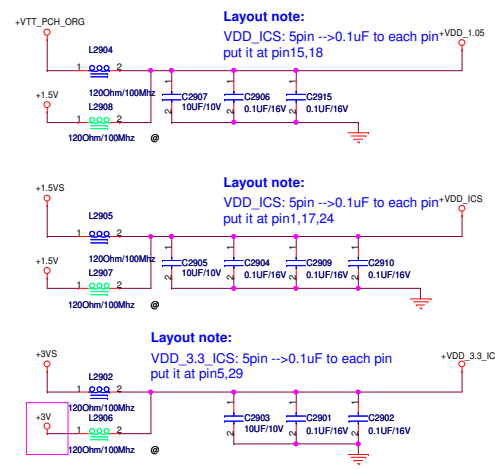
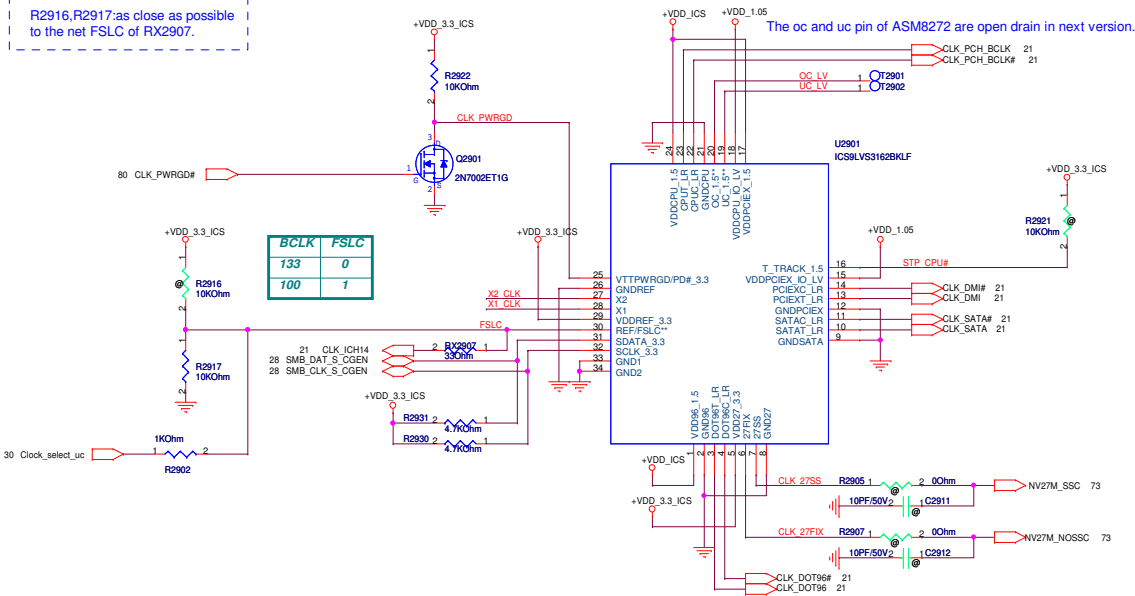
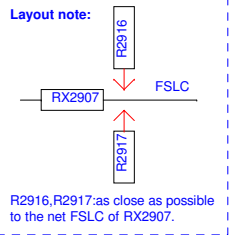
R1.2,item L6



SUBSYSTEM ID : SB_

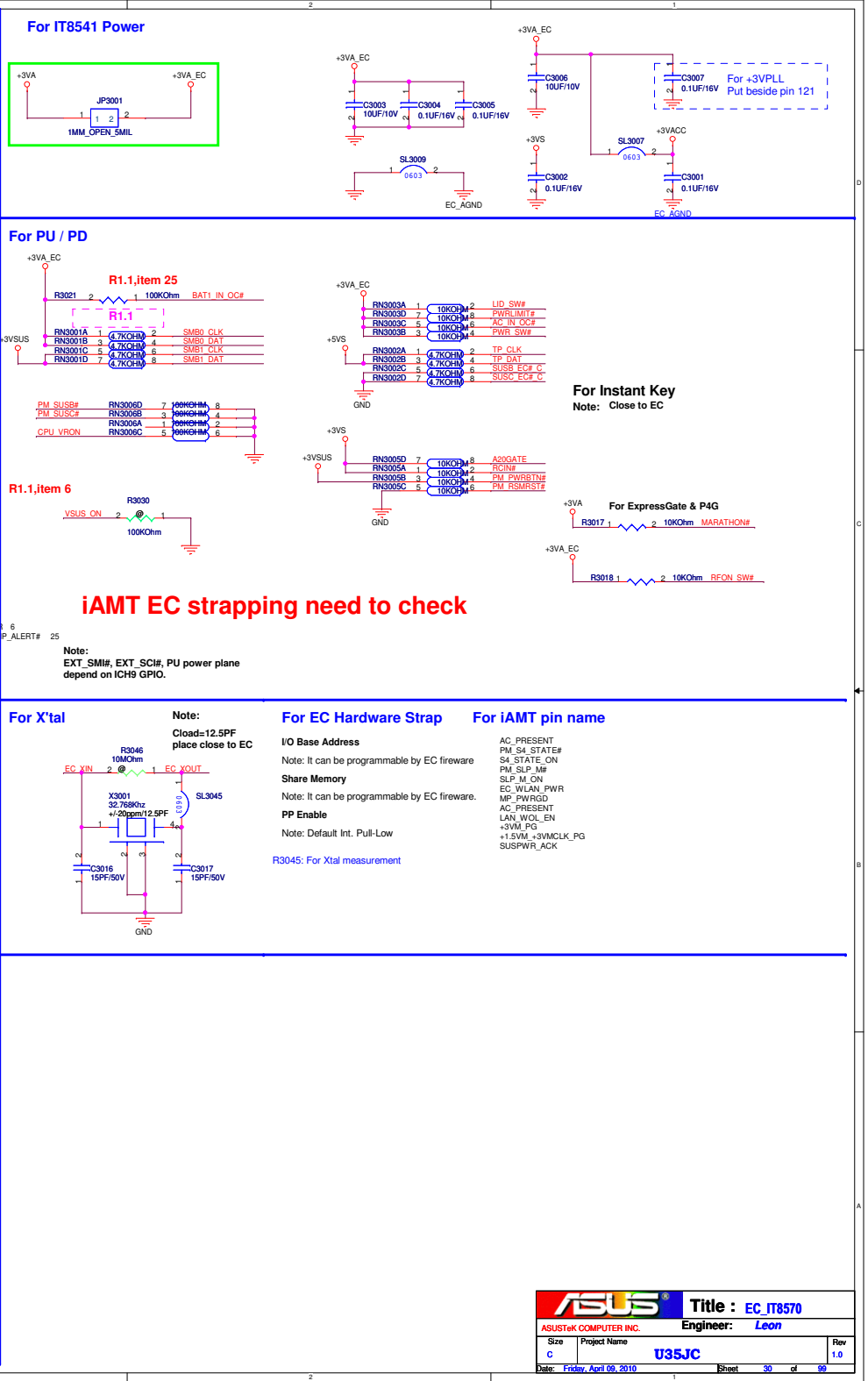
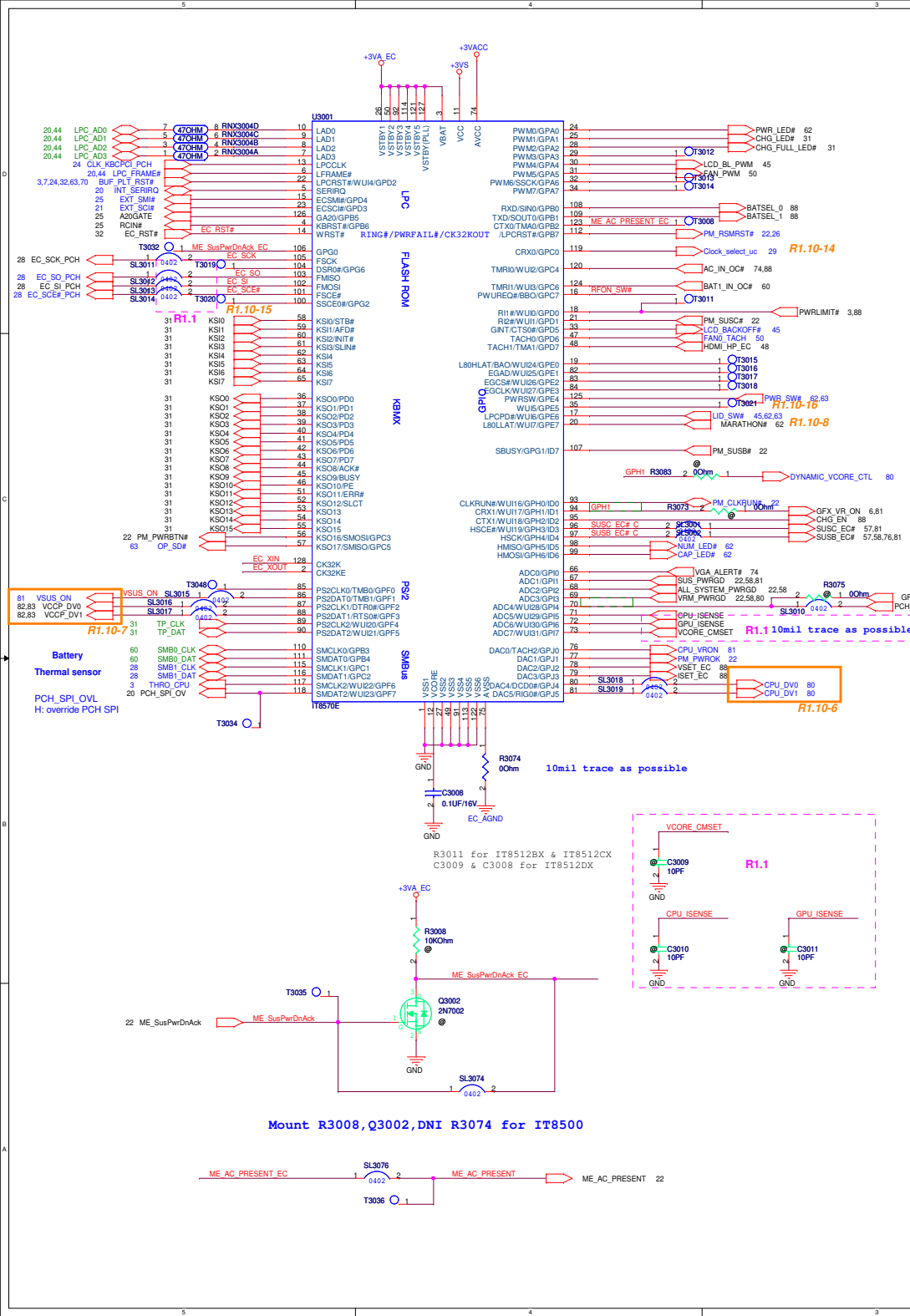
		Title : PCH_SPI ROM,OTH	
ASUSTeK COMPUTER INC. NB6		Engineer: Leon	
Size	Project Name		Rev
C	U35JC		1.0
Date: Friday, April 09, 2010		Sheet	28 of 99

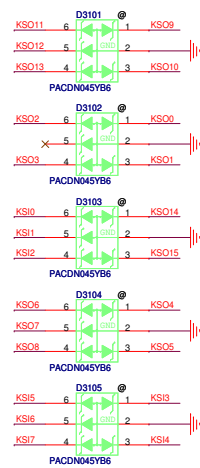
SUBSYSTEM ID : ROM



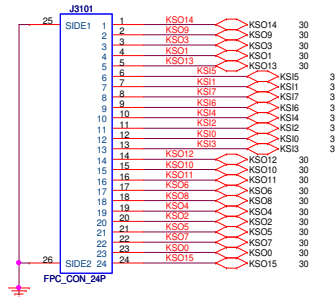
R1.10-12

R1.10-11



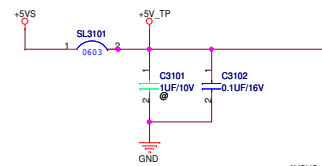


Keyboard



Layout note:
For U33JT ESD, place near J3103

Touch-Pad Conn.

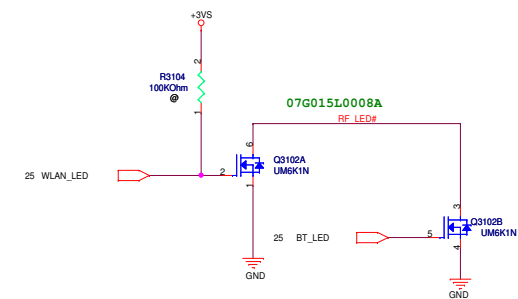


UL30JT, UL33JT colay for ME request.

IF=5mA
VF Min. 2.55V
VF Max. 3.25V
ICH9 Sink
Current Max
6mA

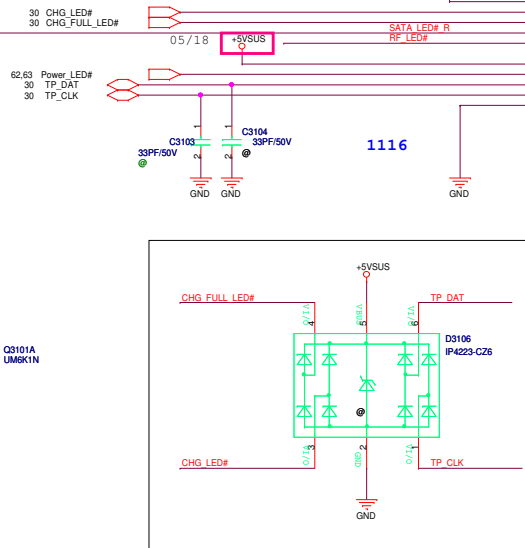
WireLess/BT LED

IF=5mA
VF Min. 2.55V
VF Max. 3.25V

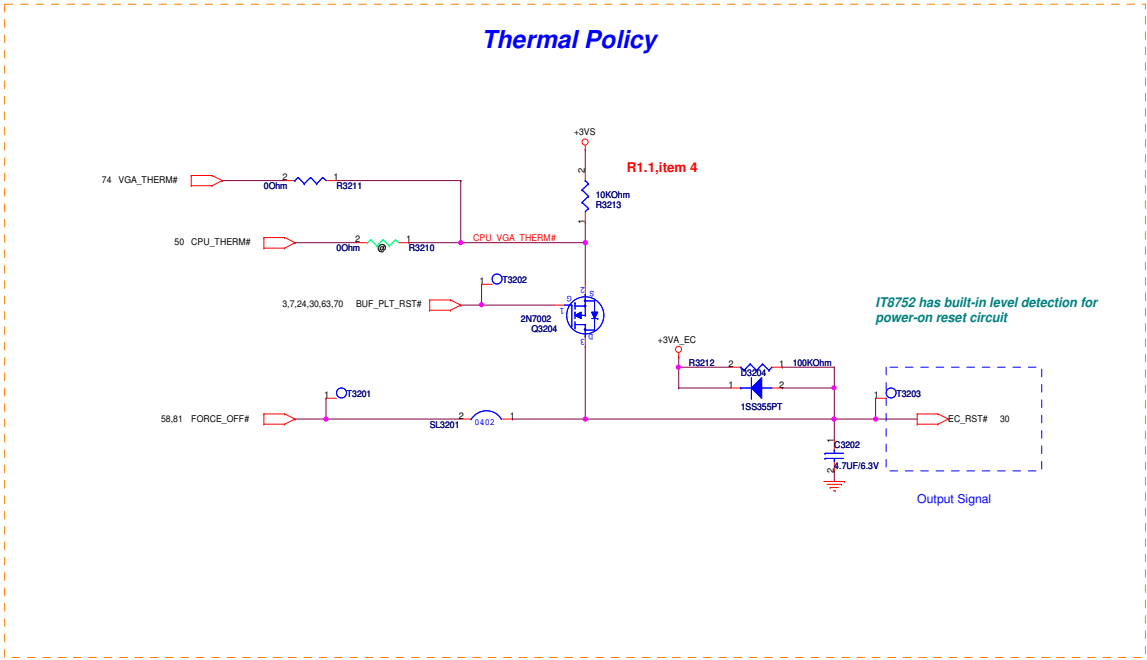


WirelessLAN & Bluetooth Status LED

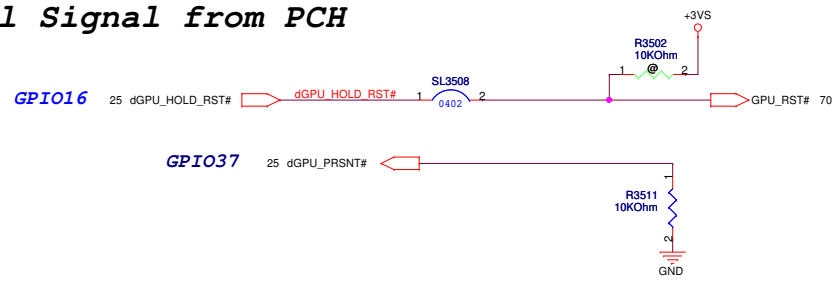
南橋只能sink 6mA



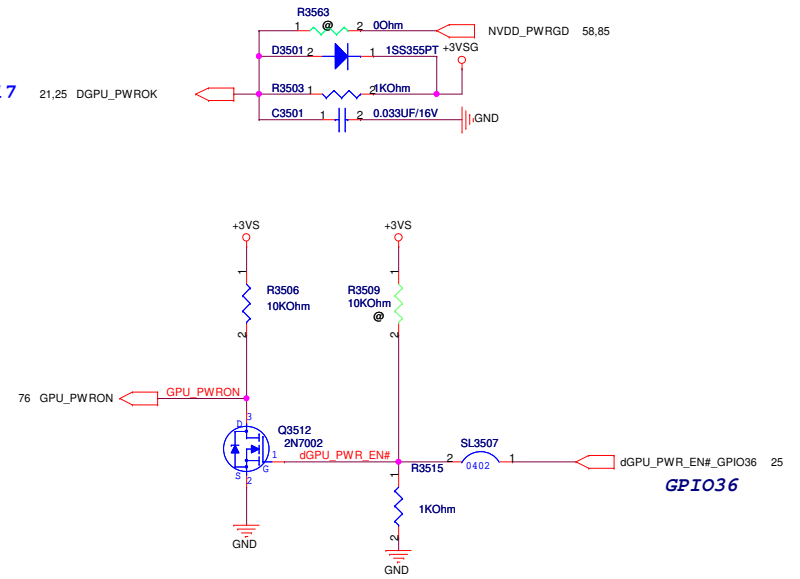
Layout note:
For UL30JT ESD, place near J3102




Control Signal from PCH



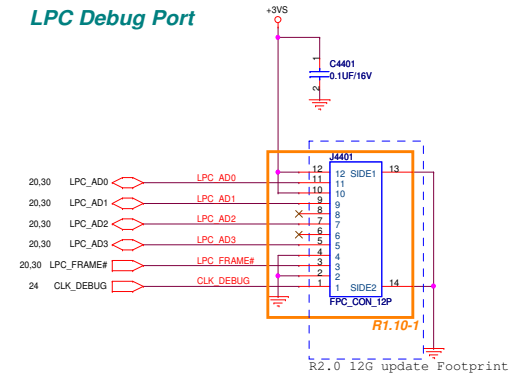
GPIO17 21,25 dGPU_PWROK



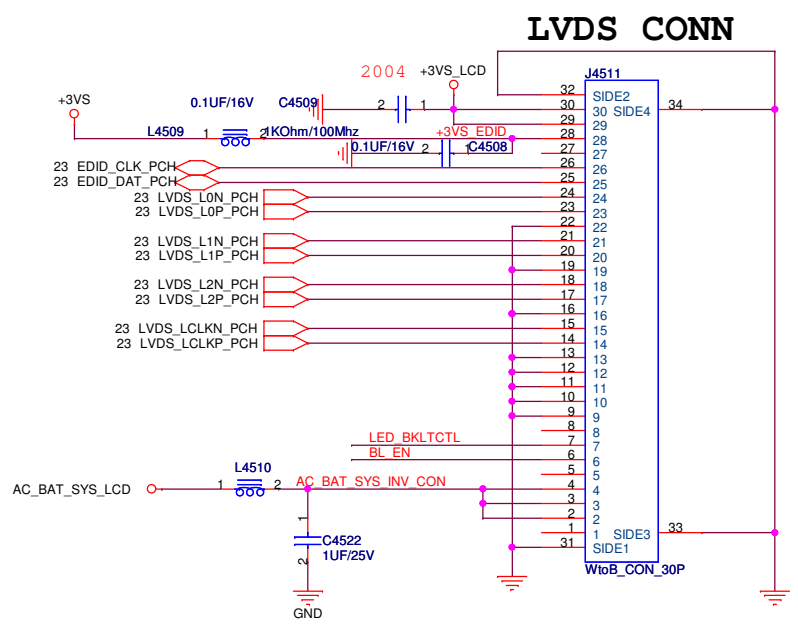
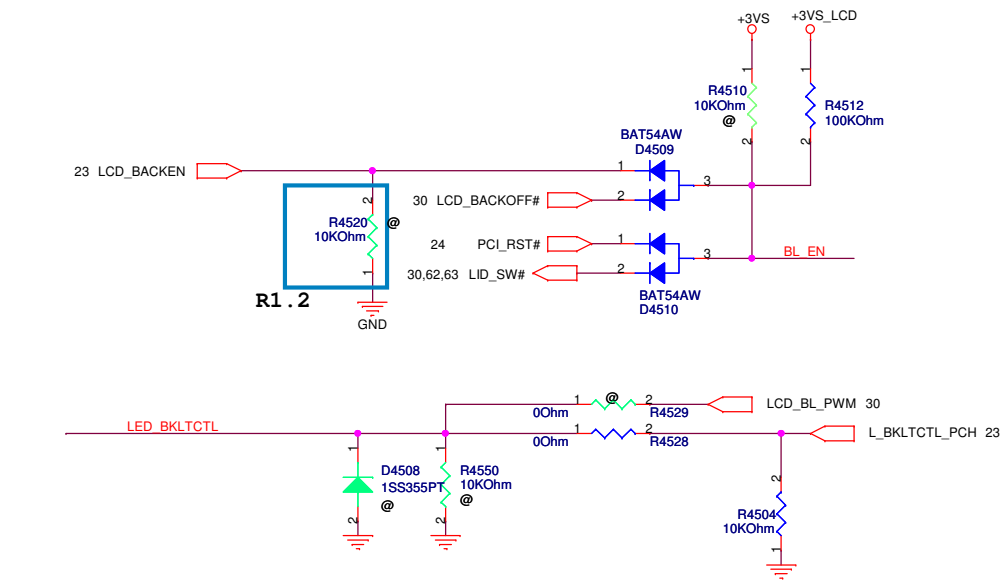
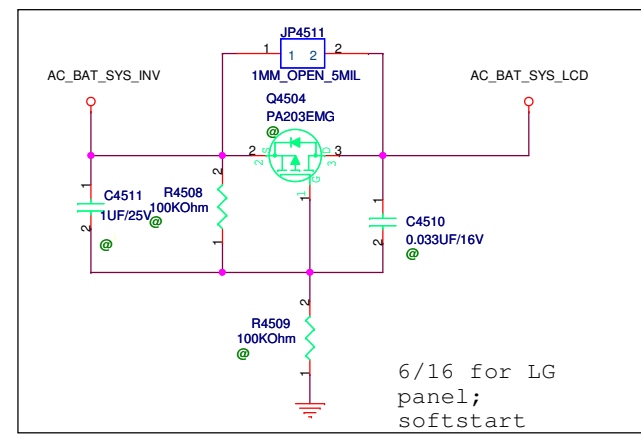
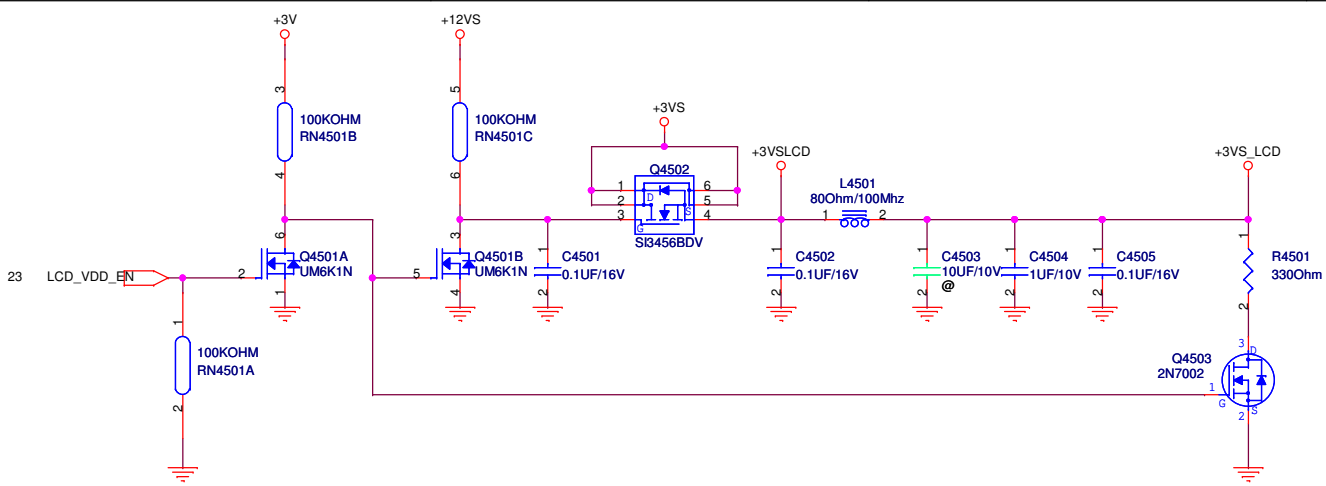
	5	4	3	2	1
D					
C					
B					
A					
	5	4	3	2	1

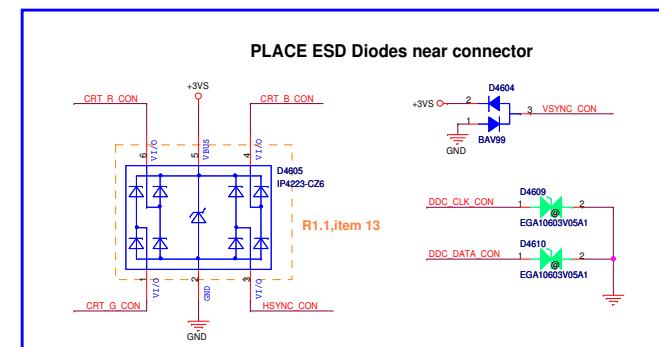
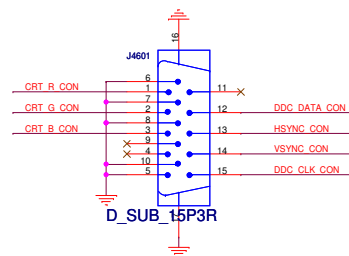
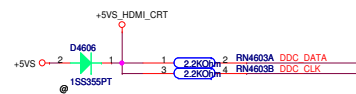
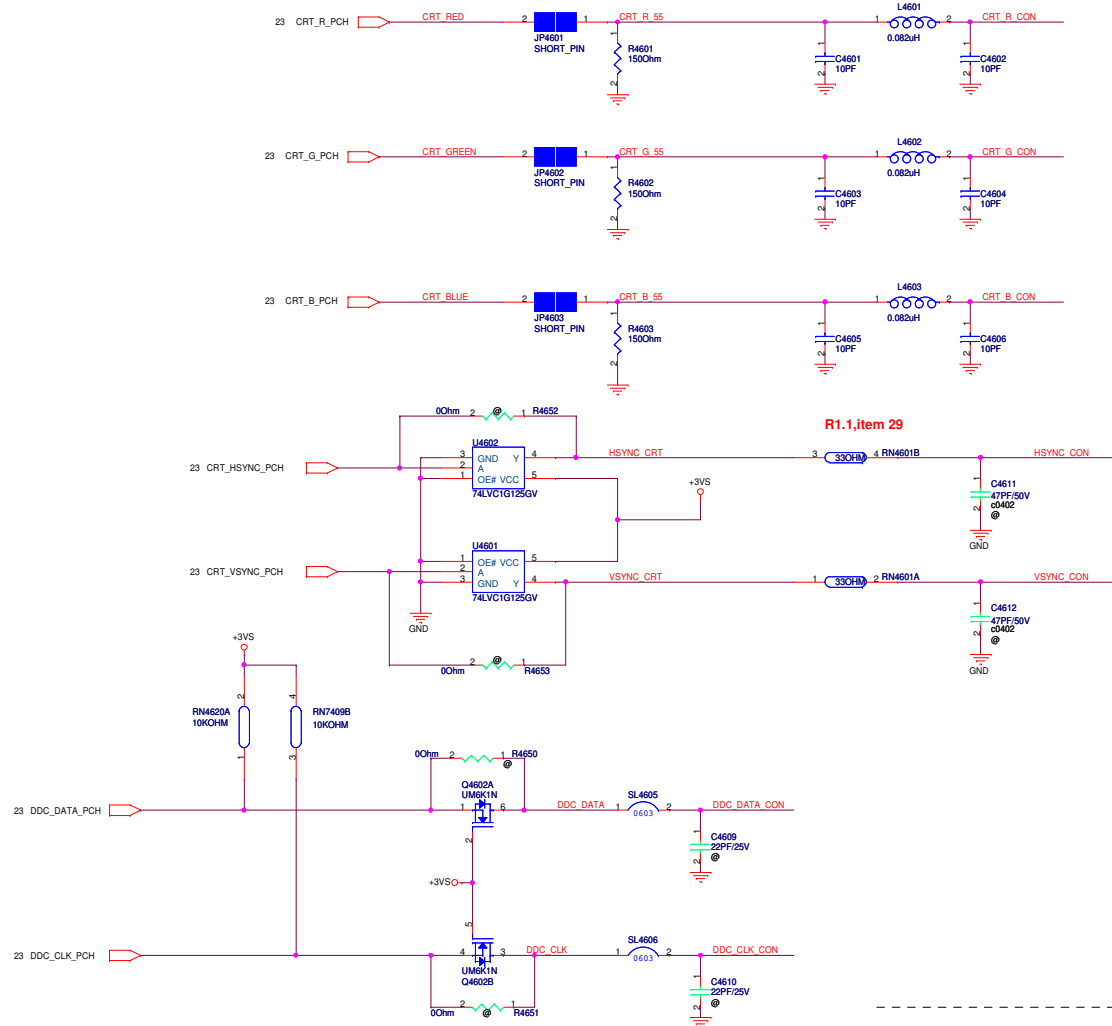
<Variant Name>		Title :	
		Engineer: <i>Leon</i>	
Size	Project Name		Rev
C	U35JC		1.0
Date:	Tuesday, March 02, 2010		Sheet 40 of 99

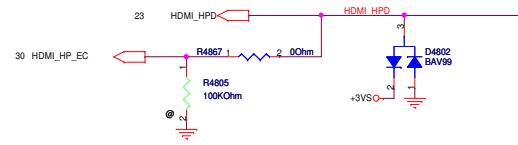
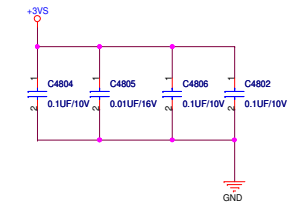
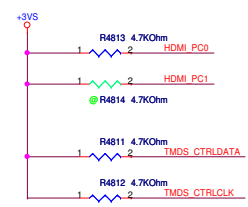
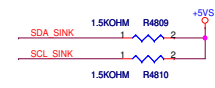
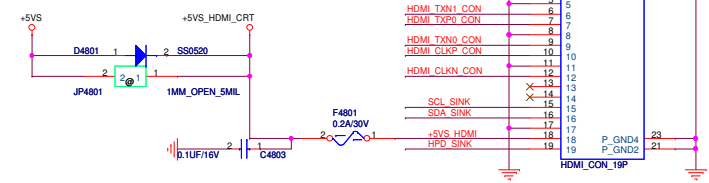
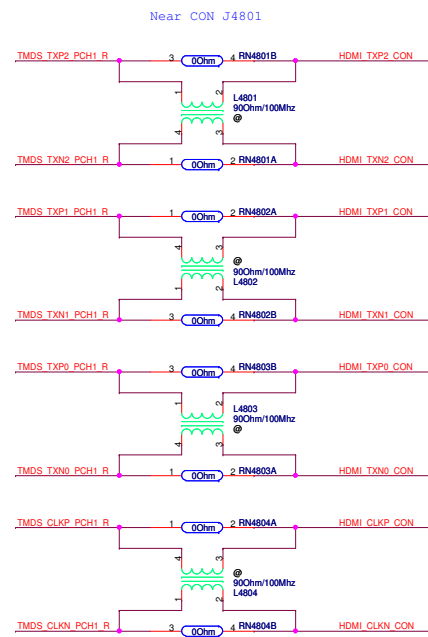
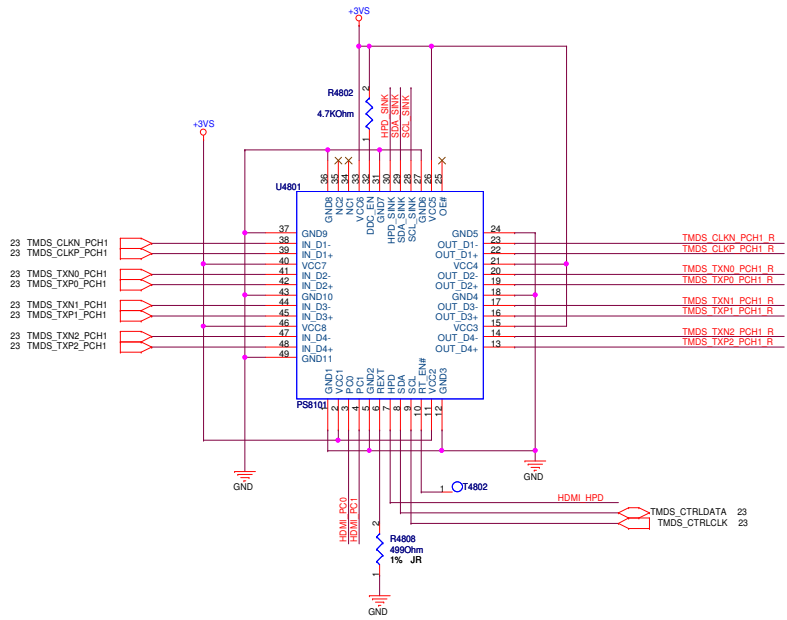
LPC Debug Port



Main Board

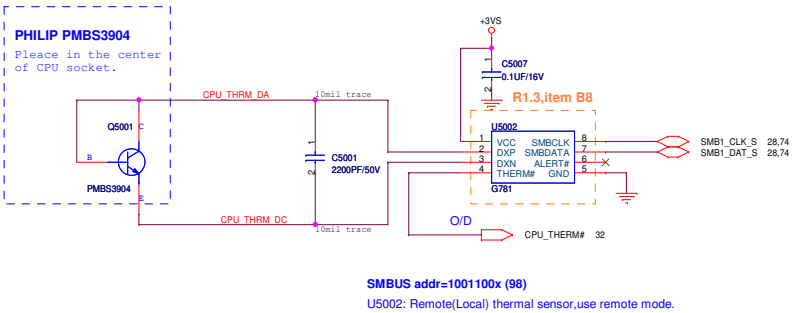






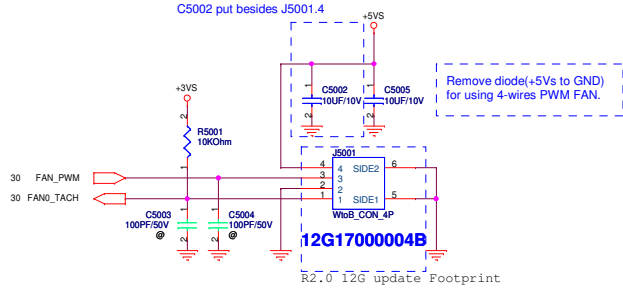
Main Board

CPU Thermal Sensor

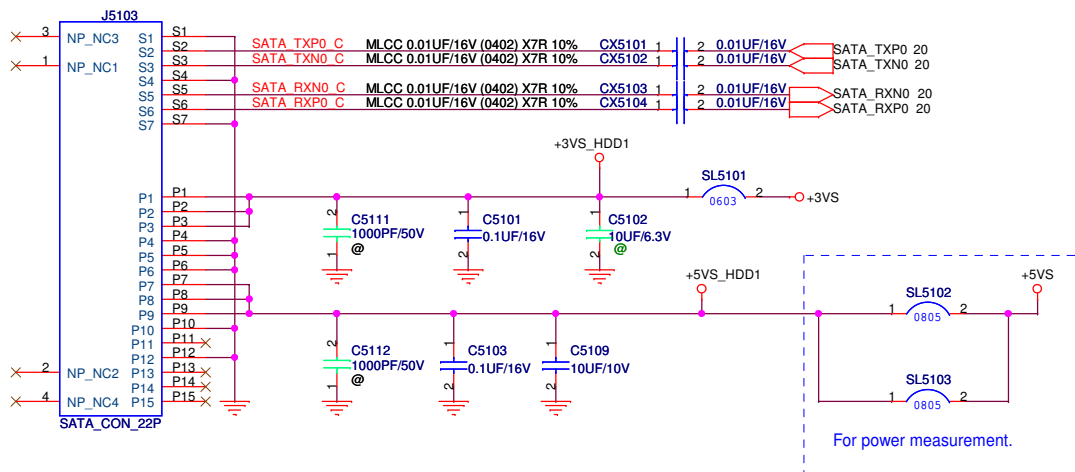


R1.10-10

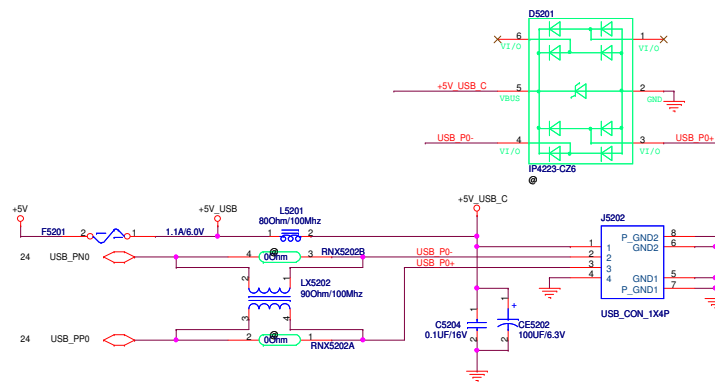
PWM Fan



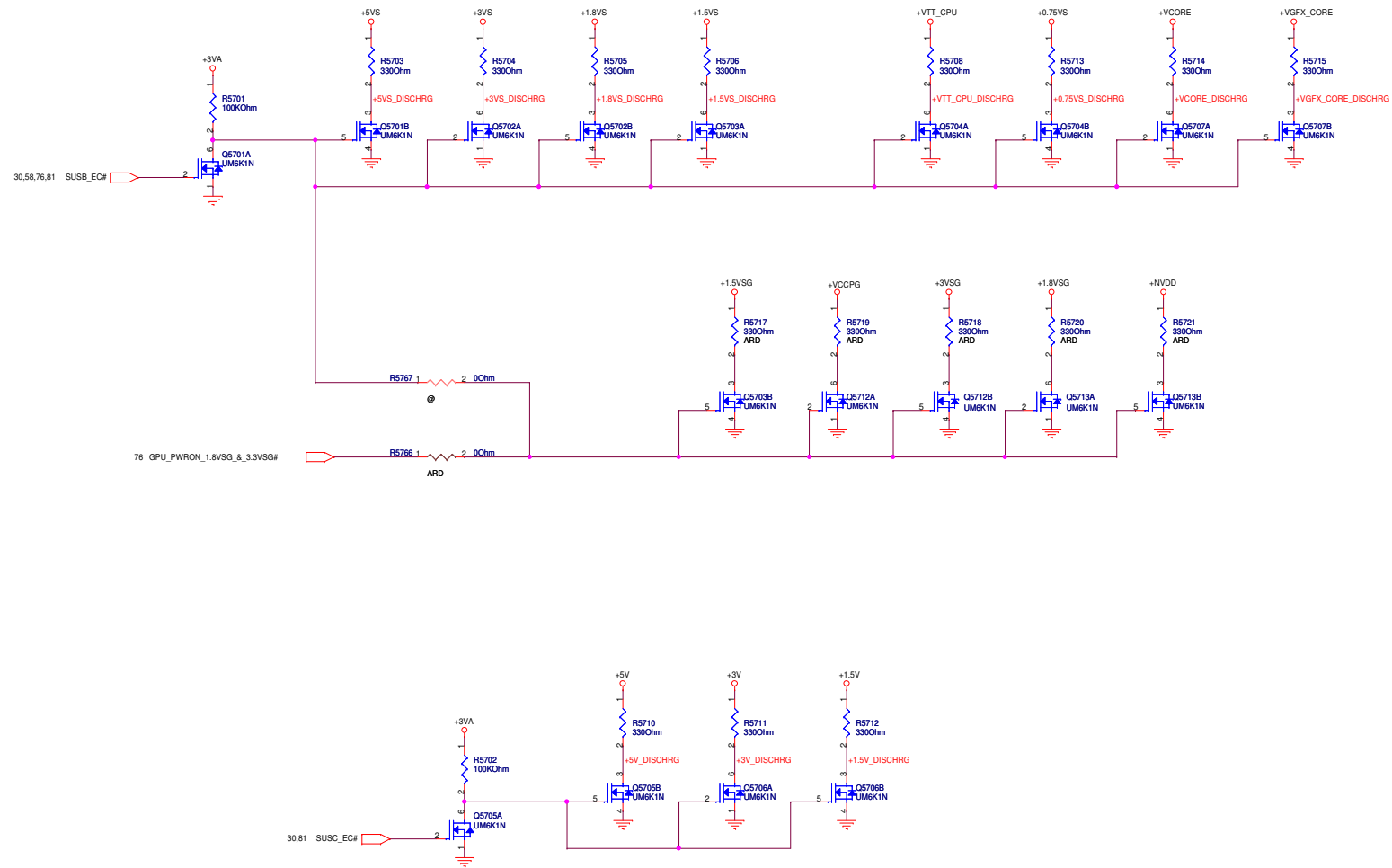
HDD (1st)



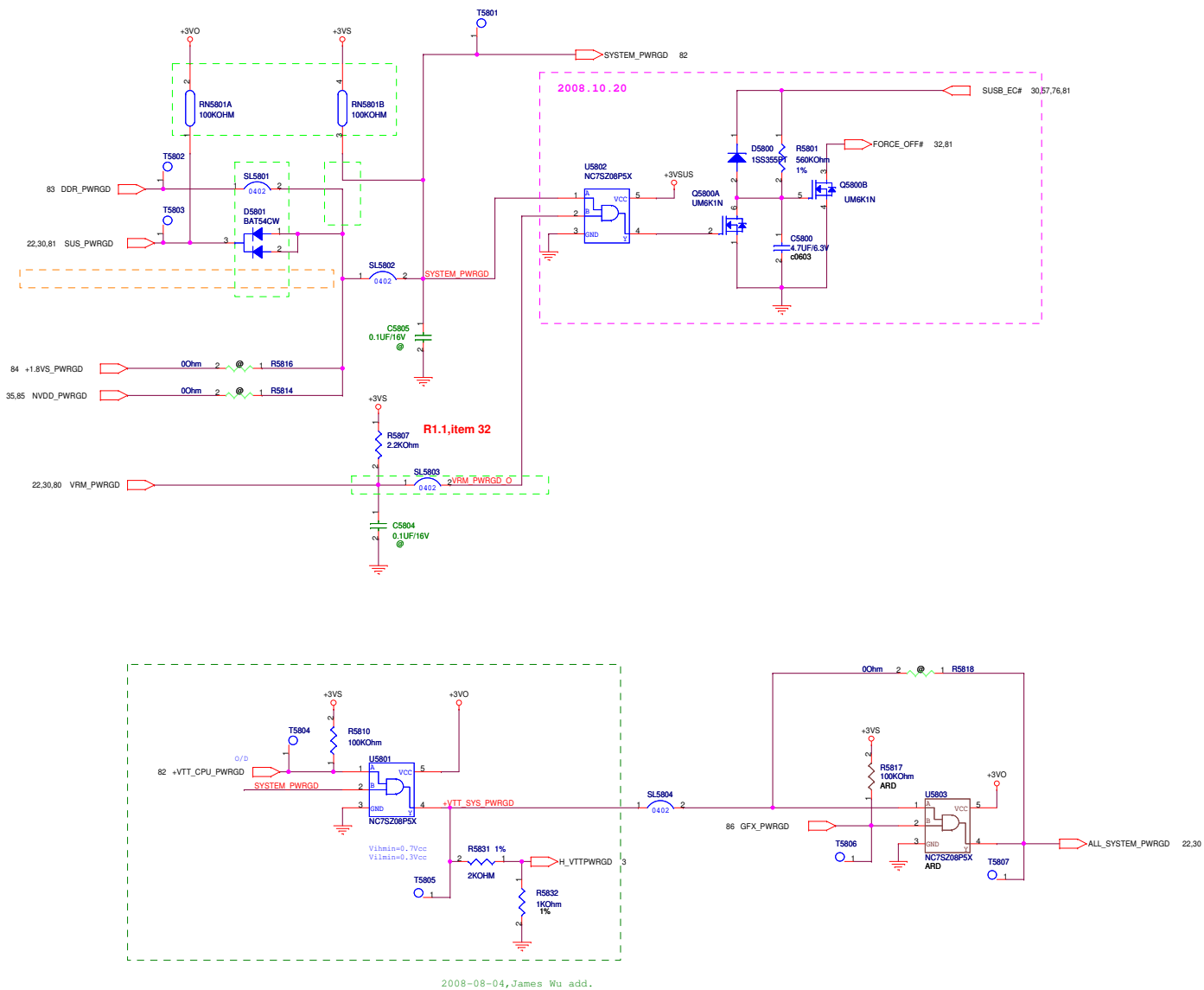
USB ports





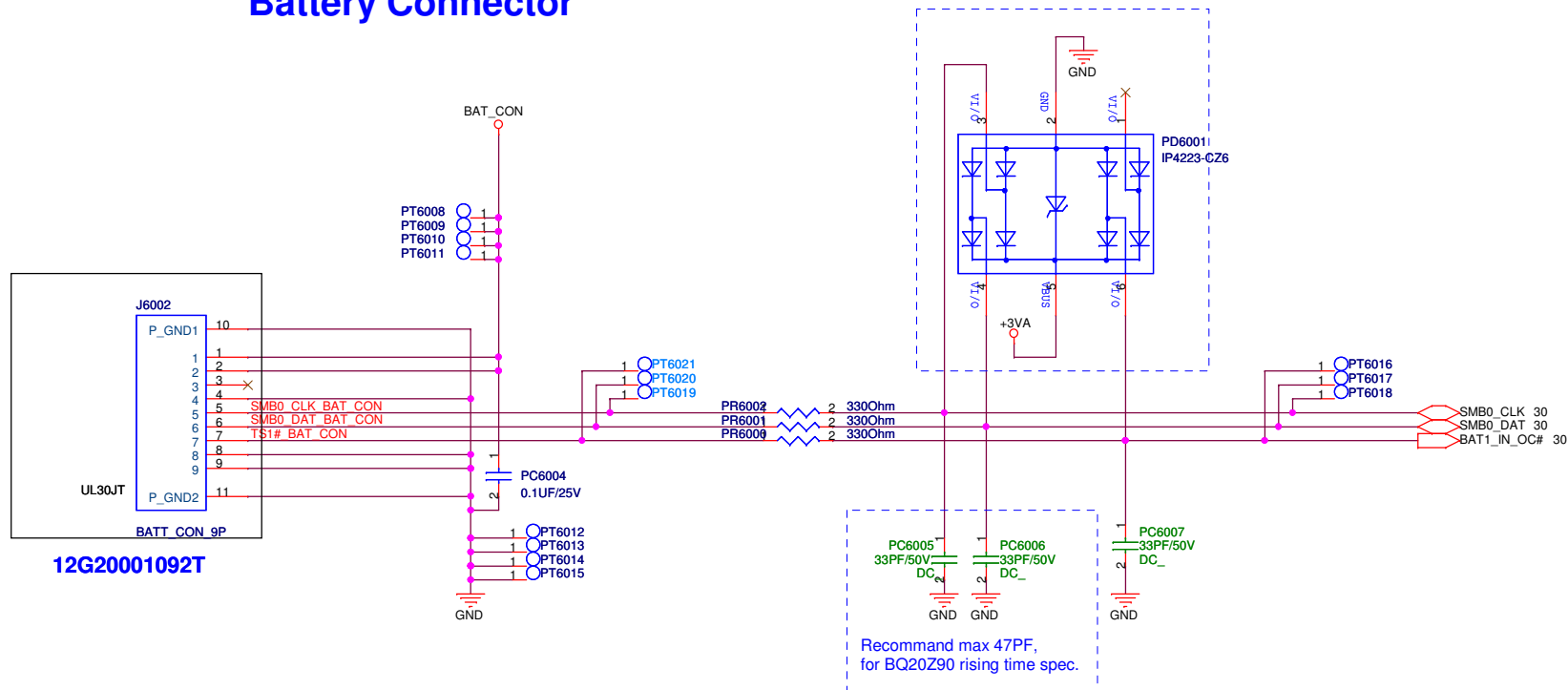


POWER GOOD DETECTOR



Main Board

Battery Connector

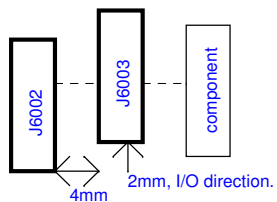


081111 -> 090604:

1. Change D6005 from DF5A6.8FU to IP4223-CZ6 for cost down and integration.

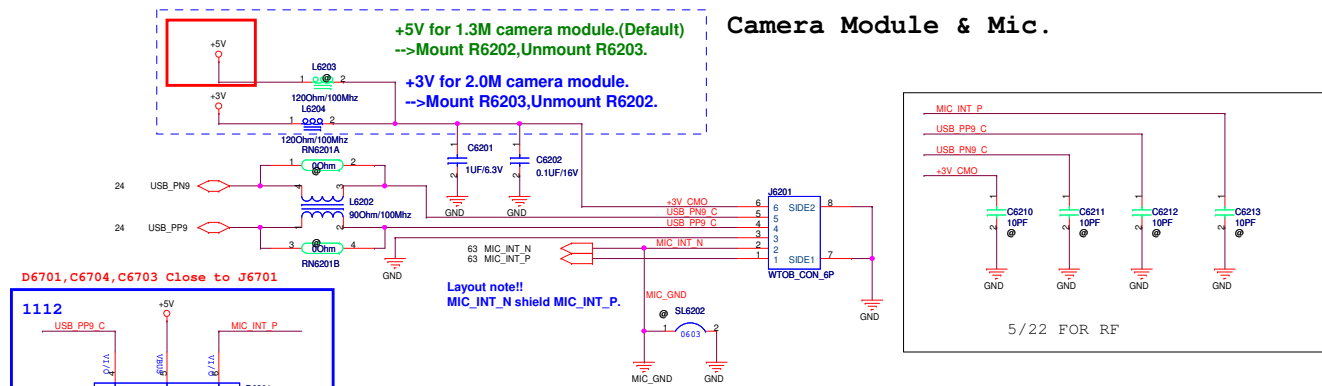
Layout note:

Battery connector colay for UL30JT & U33JT.



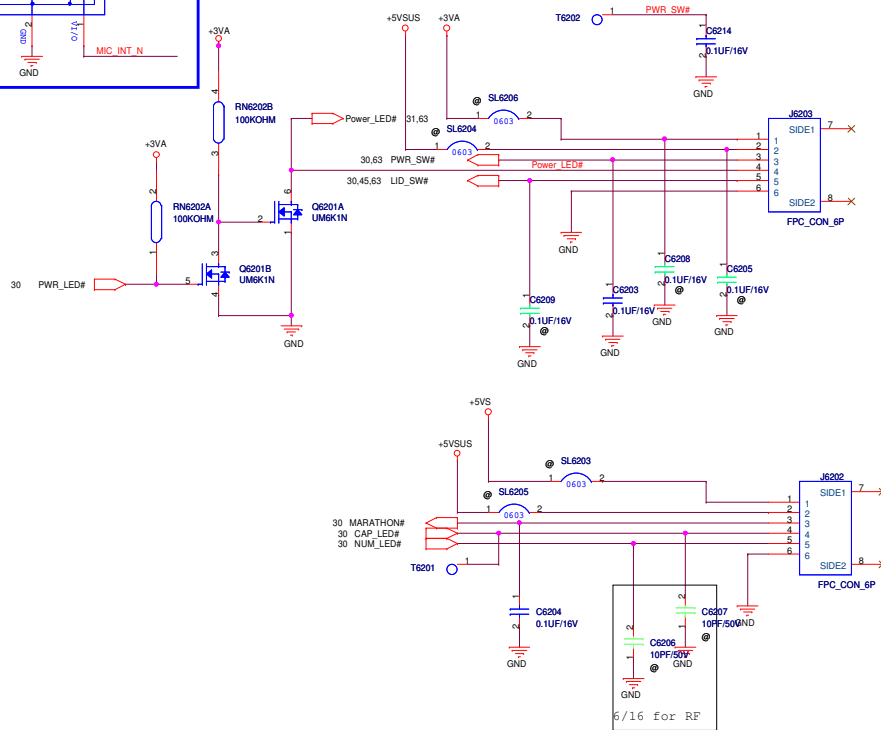
ASUS		Title :DC_BAT Conn.	
ASUSTeK COMPUTER INC. NB4		Engineer: Leon	
Size B	Project Name U35JC		Rev 1.0
Date: Friday, April 09, 2010		Sheet 60 of 99	

Camera Module & Mic.

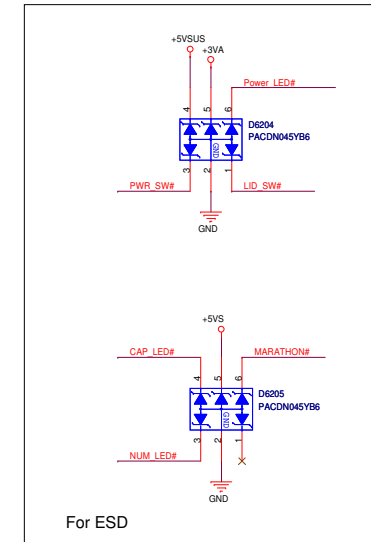


C6214: Layout add "POWER ON" text.

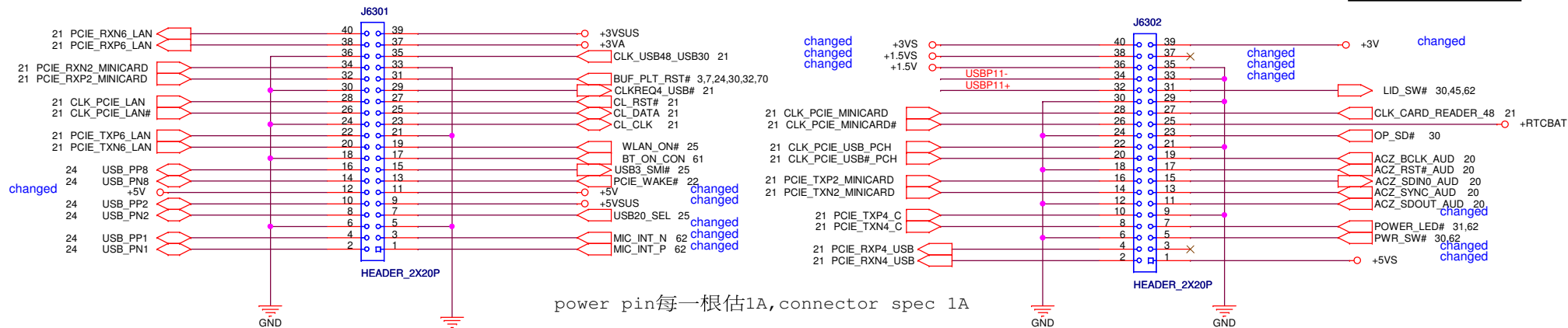
PWR S/W Board



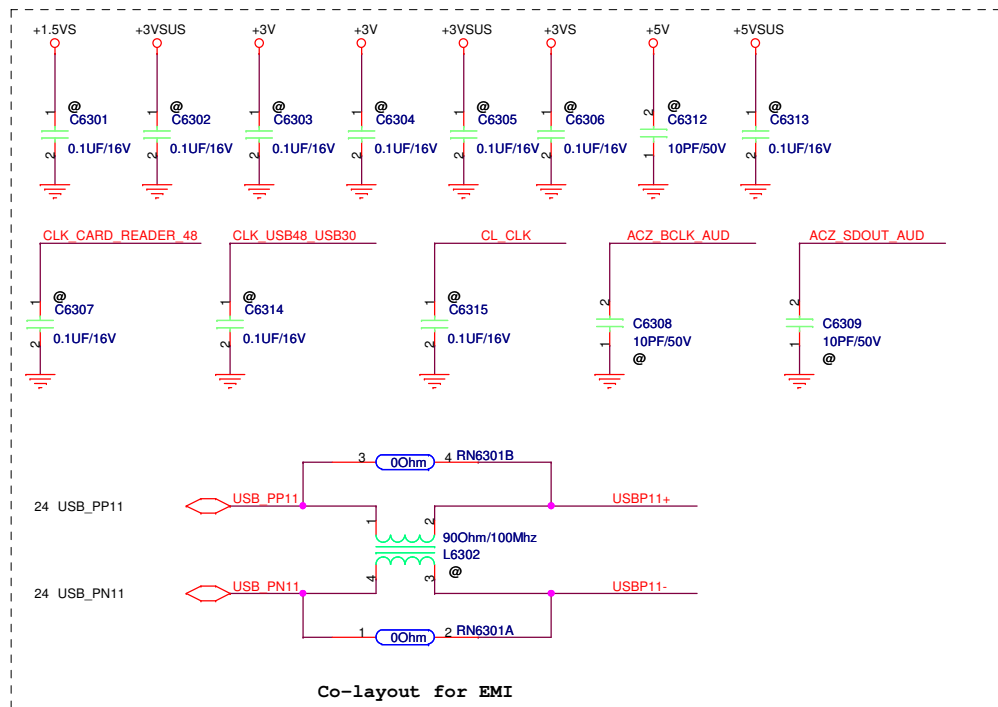
Express gate S/W Board



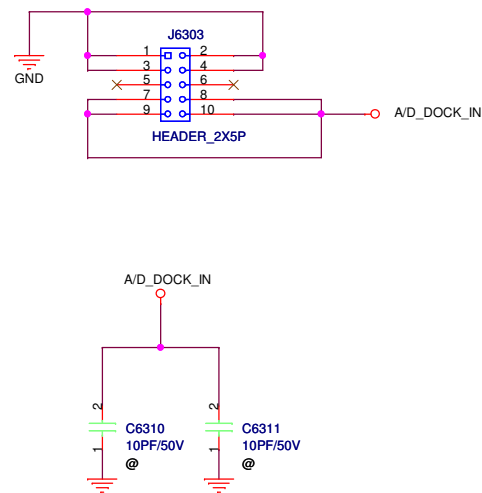
Main Board



For EMI close to connector



A/D connector

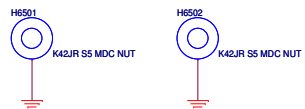


ASUS		Title : B TO B CONN	
ASUSTeK COMPUTER INC. NB4		Engineer: Leon	
Size B	Project Name U35JC		Rev 1.0
Date: Friday, April 09, 2010		Sheet 63 of 99	

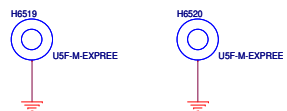
EMI spring for U33JT

Screw Hole & SMT Nut

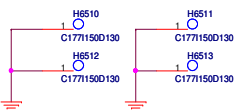
FAN NUT



GPU



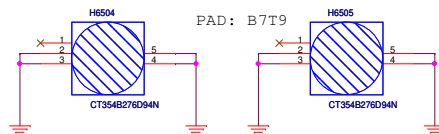
CPU



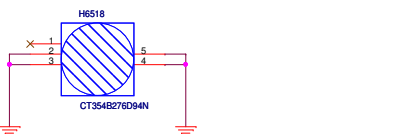
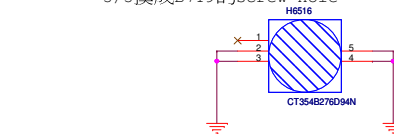
固定孔



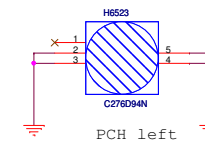
PAD: B7T9



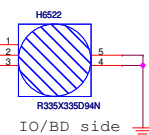
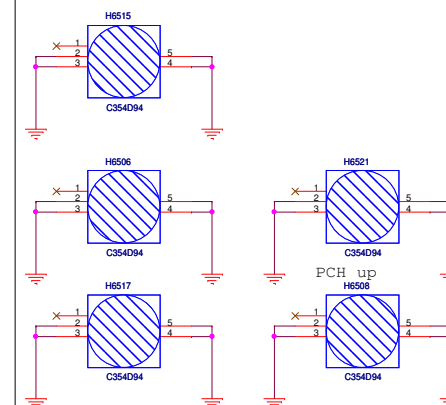
5/5换成B7T9的screw hole



PAD: B7T7




PAD: B9T9



Main Board

0.3B Beta



Title : USB 3.0_NEC (2)

ASUSTeK COMPUTER INC. NB4

Engineer: Leon

Size	Project Name	Rev
A3	U35JC	1.0

Date: Tuesday, March 02, 2010

Sheet 69 of 99

U7001C



U7001E



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nVidia DG-04131-001_V01_secured.pdf
section 9.3

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U7001F



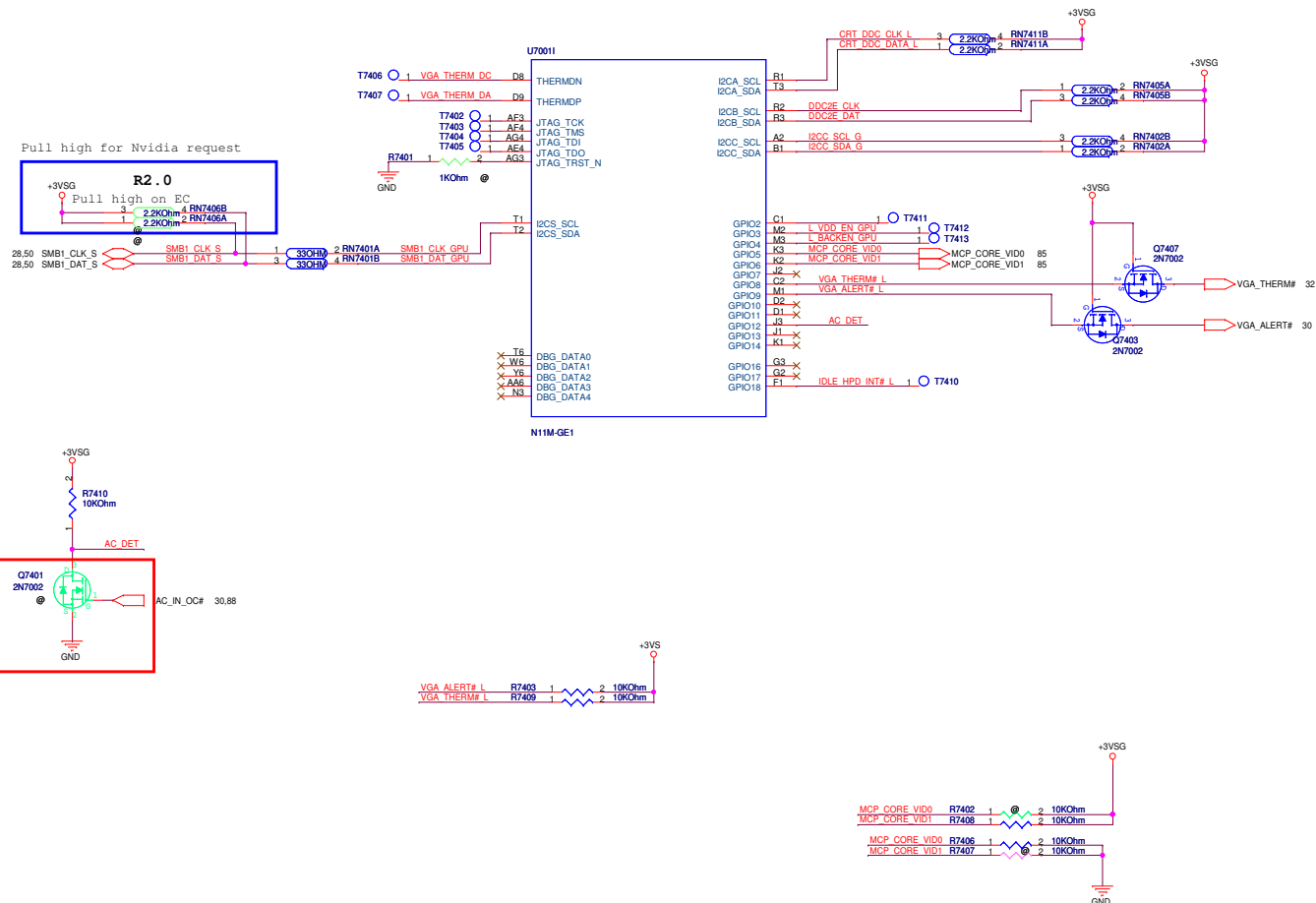
LI7001G



External thermal sensor

GPIO ASSIGNMENTS

GPIO	I/O	ACTIVE	USAGE
0	IN	N/A	NVGM
0	IN	N/A	HDMI HOTPLUG
2	OUT	HIGH	PANEL BACKLIGHT PWM
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABL
5	OUT	HIGH	NVVD VID 0
6	OUT	HIGH	NVVD VID 1
7	OUT	HIGH	FBVD VID 0
8	IN/OUT	LOW	THERMAL ALERT
9	OUT	LOW	FAN PWM
10	OUT	HIGH	FBVREF SELECT
11	OUT	HIGH	SLI SYNCO
12	IN	N/A	AC DETECT
13	OUT	LOW	PS CONTROL 0
14	OUT	HIGH	PS CONTROL 1



N10P-GE1 (N51VF)

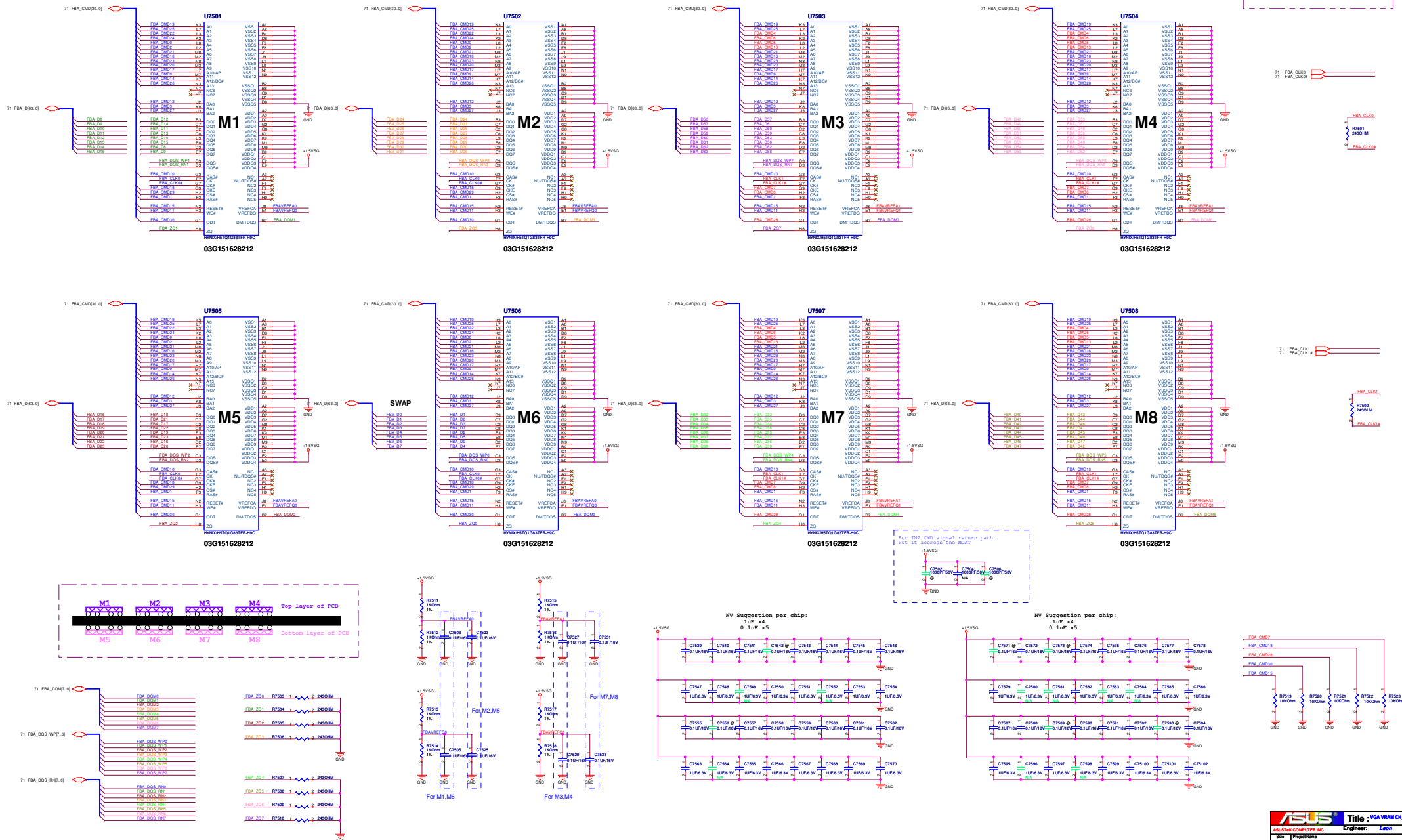
GPU_VID_0	+VGA_VCORE_0
L	0.9V
H	1.1V

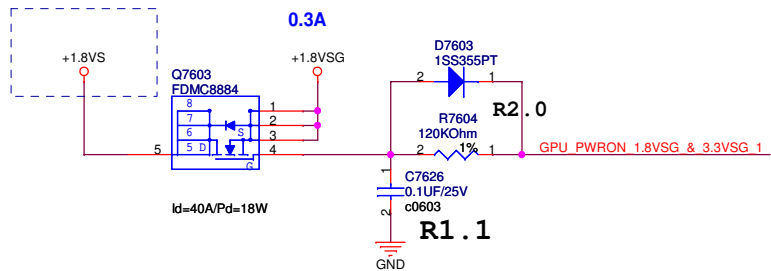
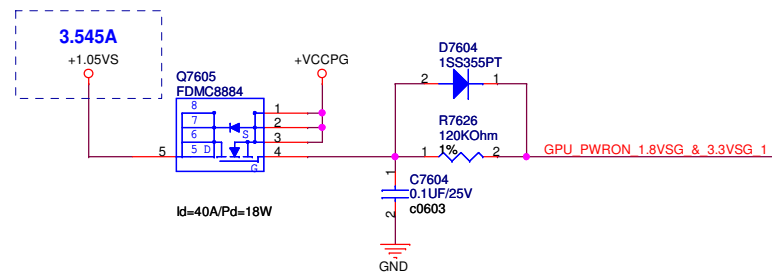
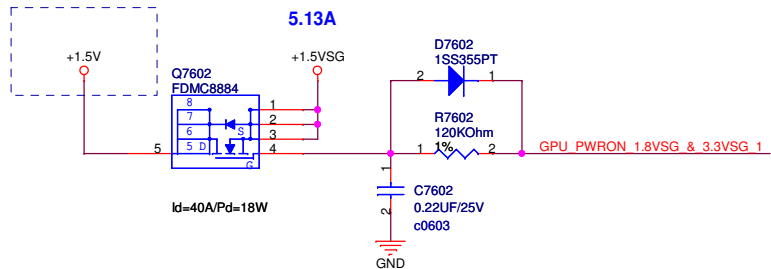
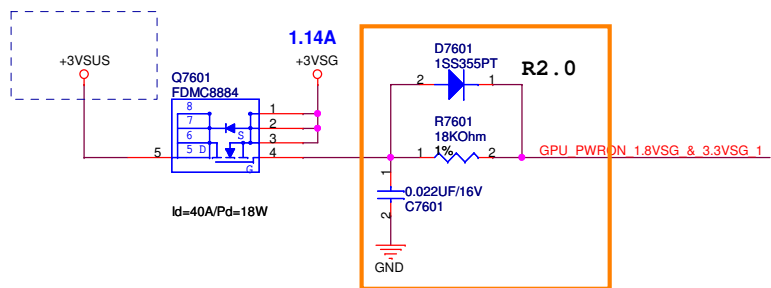
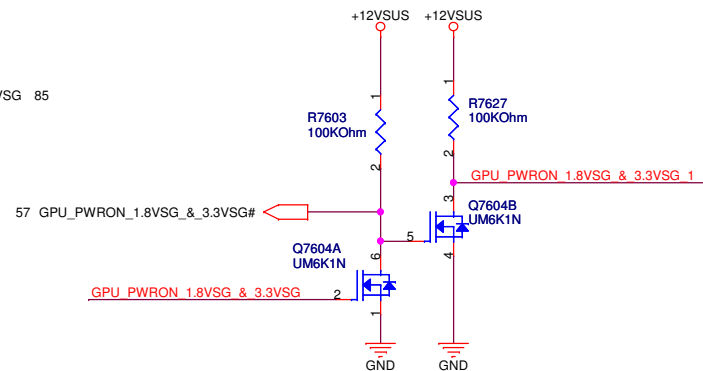
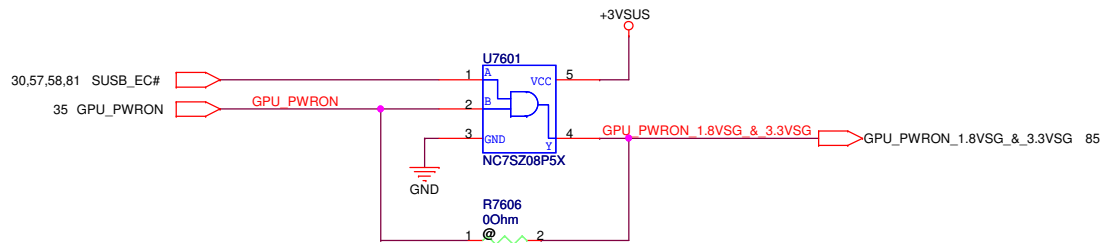
N10M-GS (N53)

GPU_VID_1	GPU_VID_0	+VGA_VCORE_0
H	L	1.0V
L	H	0.85V
L	L	0.8V

GPU_VID0	GPU_VID1	+VGA_VCORE
H	H	
H	L	1V
L	H	0.85V
L	L	0.8V

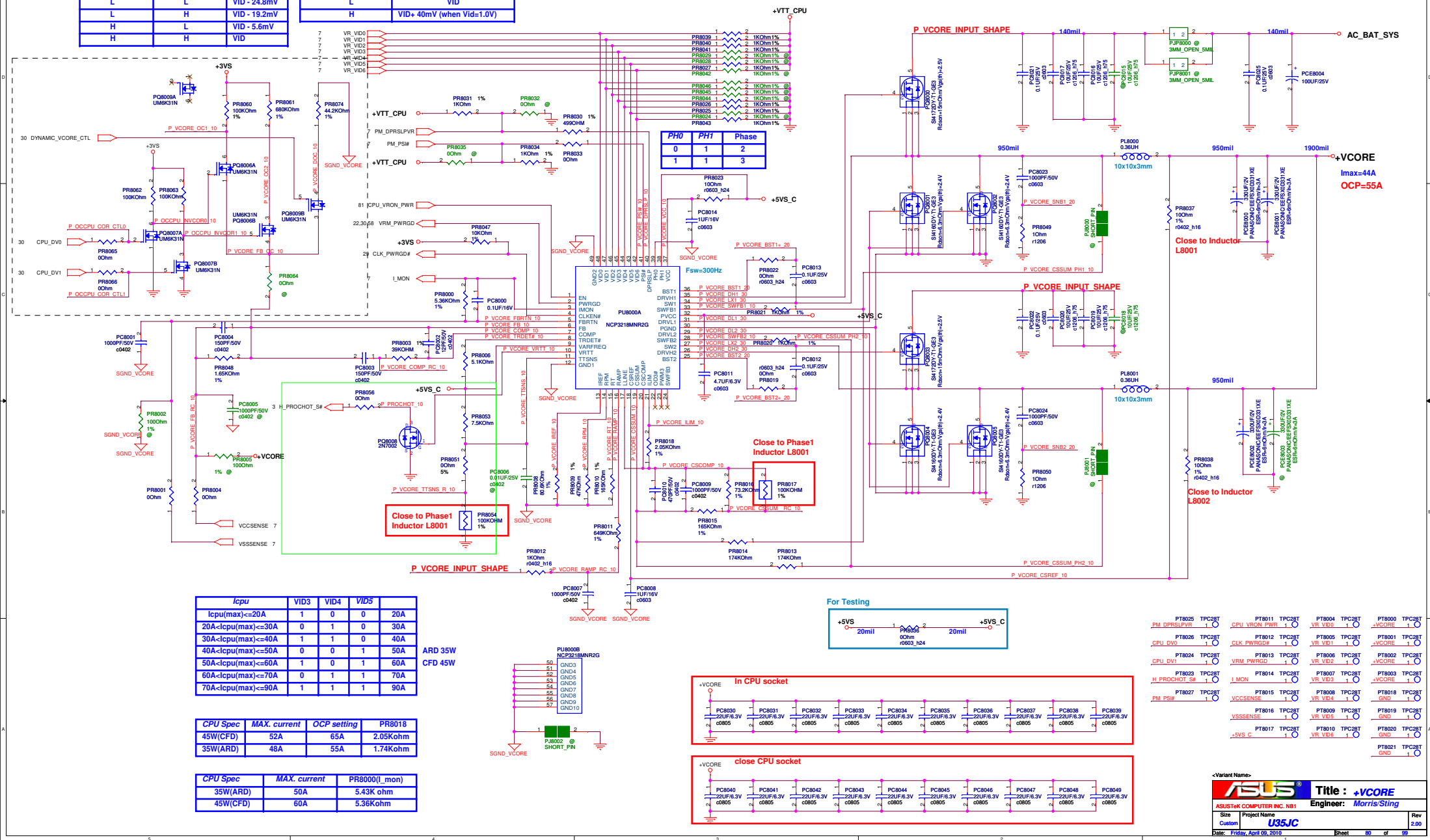
Second Source P/N:
1. 03G151628211 (Hynix)
2. 03G151628320 (Samsung)





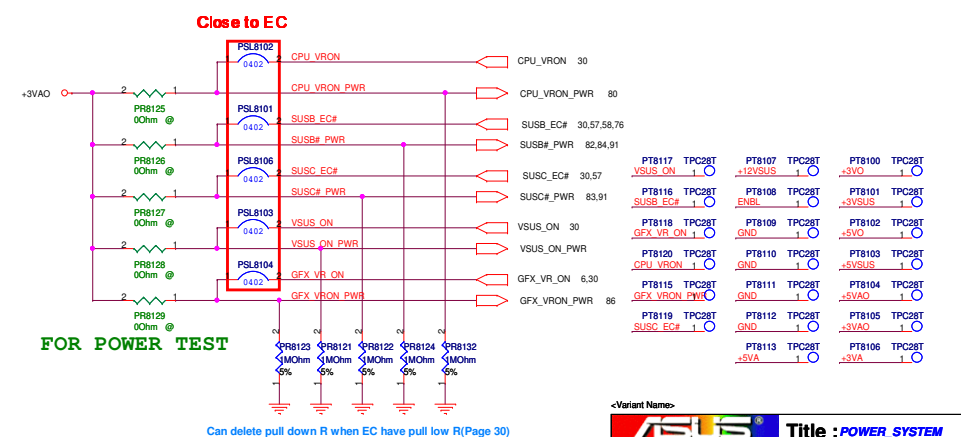
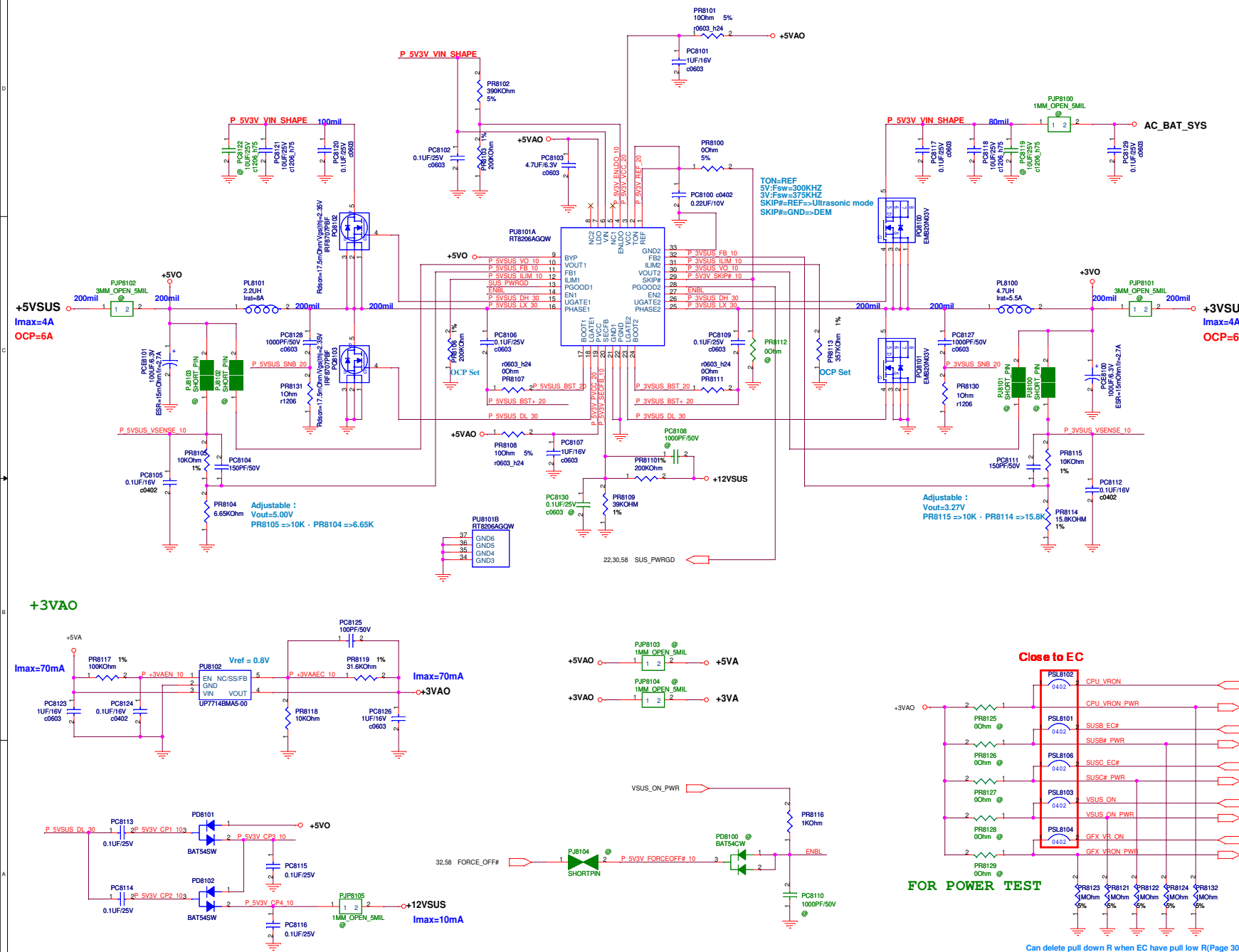
IMVP6.5 CPU VCORE REGULATOR

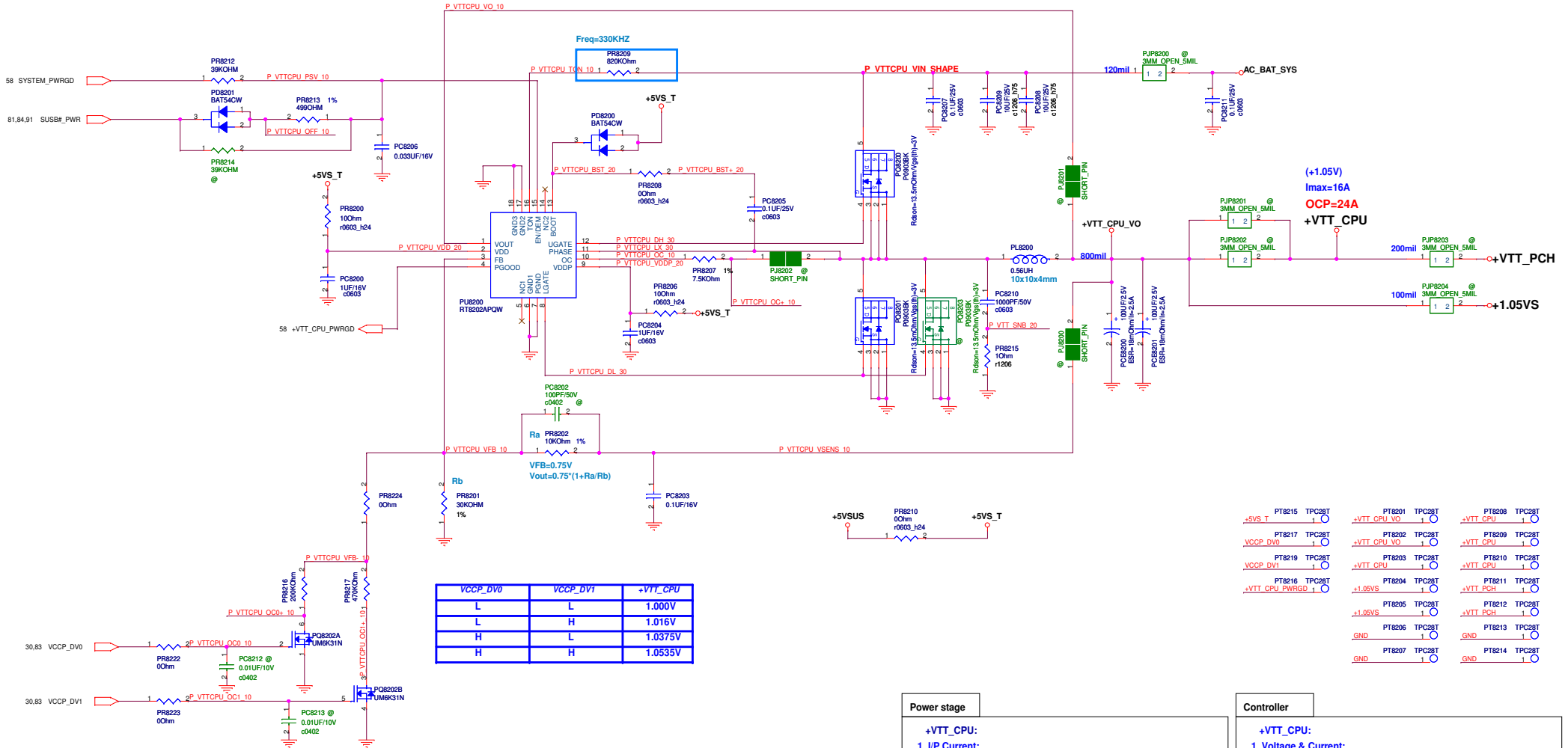
CPU_DV0	CPU_DV1	+VCORE	DYNAMIC_VCORE_DV	+VCORE
L	L	VID - 24.8mV	L	VID
L	H	VID - 19.2mV	H	VID+ 40mV (when VID=1.0V)
H	L	VID - 5.6mV		
H	H	VID		



Power stage	
+5VSUS:	+3VSUS:
1. I/P Current: $I_{in} = V_o \cdot I_o / (0.75 \cdot V_{in}) = 2.96A$	1. I/P Current: $I_{in} = V_o \cdot I_o / (0.75 \cdot V_{in}) = 1.96A$
2. Ripple Current: $I_{rip} = 2.61A$	2. Ripple Current: $I_{rip} = 1.55A$
3. Ripple Voltage: $ESR/1 = 45m\Omega$ $V = 117.45mV$	3. Ripple Voltage: $ESR/1 = 45m\Omega$ $V = 69.75mV$
4. Inductor Size: $I_{sat} = 6.2A$ $I_{dc} = 4.6A$ $DCR = 36m\Omega$	4. Inductor Size: $I_{sat} = 6.2A$ $I_{dc} = 4.6A$ $DCR = 36m\Omega$
5. MOSFET Spec:	
H-side MOSFET: FDMC8884	
$R_{ds(ON)} = 30m\Omega$	$(V_{gs} = 4.5V)$
$I_{cont} = 9A$	$(T = 25^\circ C)$
$I_{peak} = 15A$	$(Pause = 10us)$
L-side MOSFET: FDMC8884	
$R_{ds(ON)} = 30m\Omega$	$(V_{gs} = 4.5V)$
$I_{cont} = 9A$	$(T = 25^\circ C)$
$I_{peak} = 15A$	$(Pause = 10us)$

Controller	
<p>+5VSUS:</p> <p>1. Voltage & Current: +5VSUS: 5V / 4A</p> <p>2. Frequency: F=300KHZ</p> <p>3. OCP: Set R8116=357 Kohm Iocp=5uA/Rocp/10*Rs(on) Iocp=6A</p> <p>4. Soft start time: The Soft Start duration is 2ms</p> <p>5.Inrush Current: C total = 100 uF I Inrush=C*Vout/SS_time I Inrush= 0.25 A</p>	<p>+3.VSUS</p> <p>1.Voltage&Current: +3VSUS: 3.3V / 4A</p> <p>2.Frequency: F=375KHZ</p> <p>3.OCP: Set R8109=357KOhm Iocp=5uA/Rocp/10*Rs(on) Iocp=6A</p> <p>4.Inrush Current: C total = 100 uF I Inrush=C*Vout/SS_time I Inrush= 0.165 A</p>





VCCP_DV0	VCCP_DV1	+VTT_CPU
L	L	1.000V
L	H	1.016V
H	L	1.0375V
H	H	1.0535V

PT8215	TPC28T	PT8201	TPC28T	PT8208	TPC28T
+V _{SVS} T		+VTT_CPU VO		+VTT_CPU	
PT8217	TPC28T	PT8202	TPC28T	PT8209	TPC28T
+VCCP_DW0		+VTT_CPU VO		+VTT_CPU	
PT8219	TPC28T	PT8203	TPC28T	PT8210	TPC28T
+VCCP_DW1		+VTT_CPU		+VTT_CPU	
PT8216	TPC28T	PT8204	TPC28T	PT8211	TPC28T
+VTT_CPU_PWRRD ₁		+1.05VS		+VTT_PCH	
		PT8205	TPC28T	PT8212	TPC28T
		+1.05VS		+VTT_PCH	
		PT8206	TPC28T	PT8213	TPC28T
		GND		GND	
		PT8207	TPC28T	PT8214	TPC28T
		GND		GND	

Power stage

+VTT_CPU:

1. **IP Current:**
 $I_{in} = V_o / I_o (0.75 \cdot V_{in}) = 2.33A$
2. **Ripple Current:**
 $I_{rip} = 9.18A$
3. **Ripple Voltage:**
 $ESR/2 = 7.5m\Omega$
 $V = 68.85mV$
4. **Inductor Spec:**
 $I_{sat} = 29.1A$
 $I_{dc} = 26A$
 $DCR = 1m\Omega$
5. **MOSFET Spec:**
H-side MOSFET: RJK0355DPA

 $R_{ds(ON)} = 16.5m\Omega$ ($V_{gs} = 4.5V$)
 $I_{cont} = 30A$ ($T = 25^\circ C$)
 $I_{peak} = 120A$ (Pause = 10 μs)

L-side MOSFET: RJK0353DPA

Rds(ON)=7.6mohm (Vgs=4.5 V)
I cont = 35A (T=25 °C)
I peak =140 A (Pause =10 us)

Controller

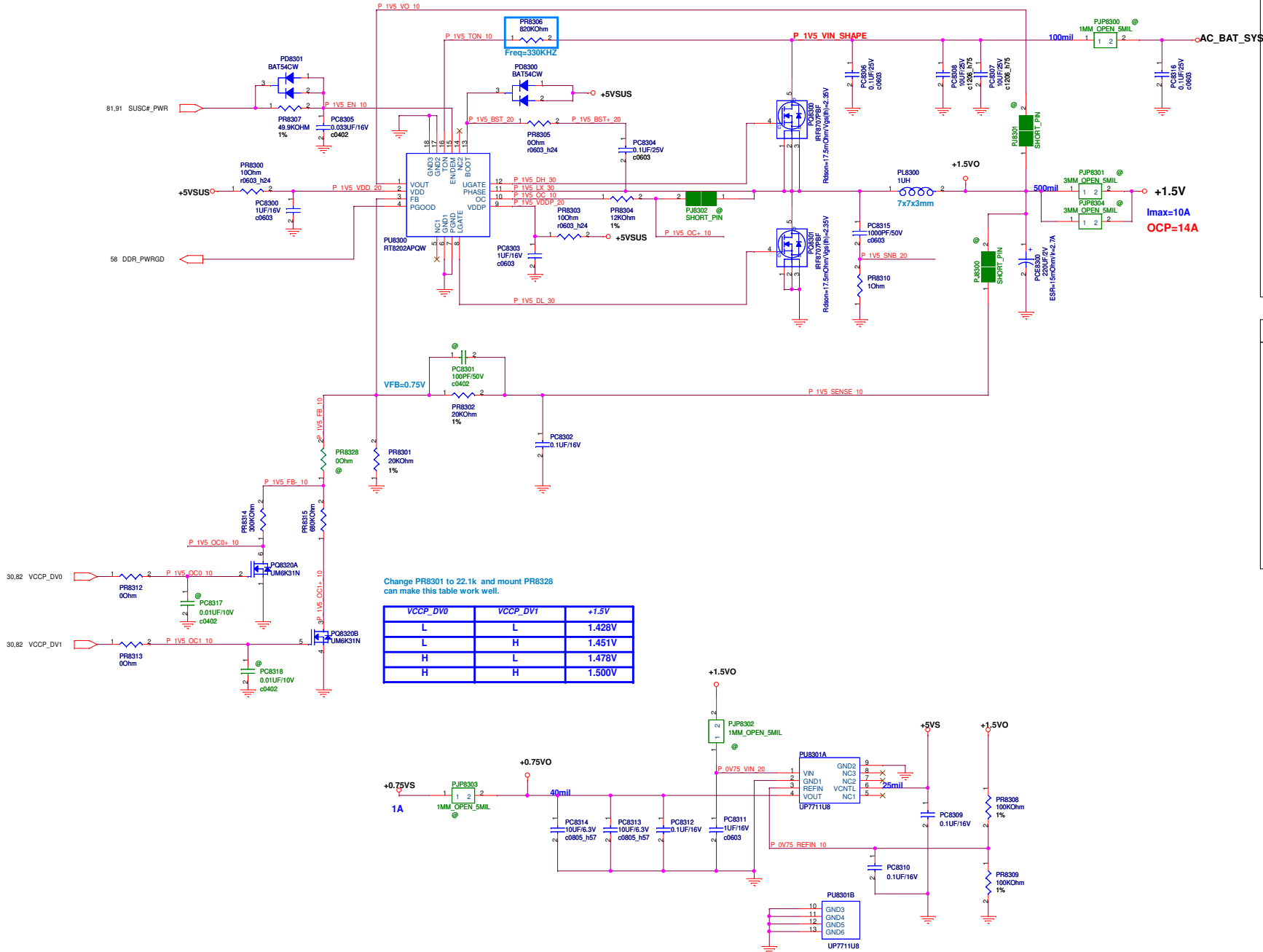
+VTT_CPU:

1. **Voltage & Current:**
+VTT_CPU: 1.05V / 15A
2. **Frequency:**
F=300KHZ
3. **OCP:**
Set R802=4.99 Kohm
Iocp=Rocp*20uA/Rds(on)
Iocp=26A
4. **Soft start time:**
The SS duration is 1.35ms
5. **Inrush Current:**
C total = 440 uF
I inrush=C*Vout/SS_time
I inrush= 0.342 A

<Variant Name>



+1.5V & +0.75VS POWER SUPPLY



Power stage

DDR III:

1. I/P Current:

$I_{in} = V_o \cdot I_o / (0.75 \cdot V_{in}) = 2.22A$

2. Ripple Current:

$I_{rip} = 4.62A$

3. Ripple Voltage:

$ESR = 1 = 15m\Omega$
 $V = 69.3mV$

4. Inductor Spec:

$I_{sat} = 12.7A$
 $I_{dc} = 9.5A$
 $DCR = 8.5m\Omega$

5. MOSFET Spec:

H-side MOSFET: RJK0355DPA

$R_{ds(ON)} = 16.5m\Omega$ ($V_{gs} = 4.5V$)
 $I_{cont} = 30A$ ($T = 25^\circ C$)
 $I_{peak} = 120A$ (Pause = 10 us)

L-side MOSFET: RJK0355DPA

$R_{ds(ON)} = 16.5m\Omega$ ($V_{gs} = 4.5V$)
 $I_{cont} = 30A$ ($T = 25^\circ C$)
 $I_{peak} = 120A$ (Pause = 10 us)

Controller

DDR III:

1. Voltage & Current:

+1.5V: 1.5V / 10A

+0.75V: 0.75V / 1A

2. Frequency:

$F = 300KHZ$

3. OCP:

Set R8302=12 Kohm
 $I_{ocp} = R_{ocp} \cdot 20uA / R_{ds(on)}$
 $I_{ocp} = 14.3A$

4. Soft start time:

The Soft Start duration is 1.35ms

5. Inrush Current:

$C_{total} = 220uF$
 $I_{inrush} = C \cdot V_{out} / SS_time$
 $I_{inrush} = 0.244A$

Change PR8301 to 22.1k and mount PR8328 can make this table work well.

VCCP_DV0	VCCP_DV1	+1.5V
L	L	1.428V
L	H	1.451V
H	L	1.478V
H	H	1.500V

PT8300 TPC28T
+1.5VQ 1
PT8301 TPC28T
+1.5VQ 1
PT8302 TPC28T
+1.5V 1
PT8303 TPC28T
+1.5V 1
PT8304 TPC28T
+0.75VQ 1
PT8305 TPC28T
+0.75VS 1
PT8306 TPC28T
GND 1
PT8307 TPC28T
GND 1
PT8308 TPC28T
GND 1
PT8309 TPC28T
GND 1

<Variant Name>

ASUS

Title : POWER_I/O_DDR

ASUSTeK COMPUTER INC. NB

Engineer: Morris/Sting

Size

Project Name

Rev

Custom

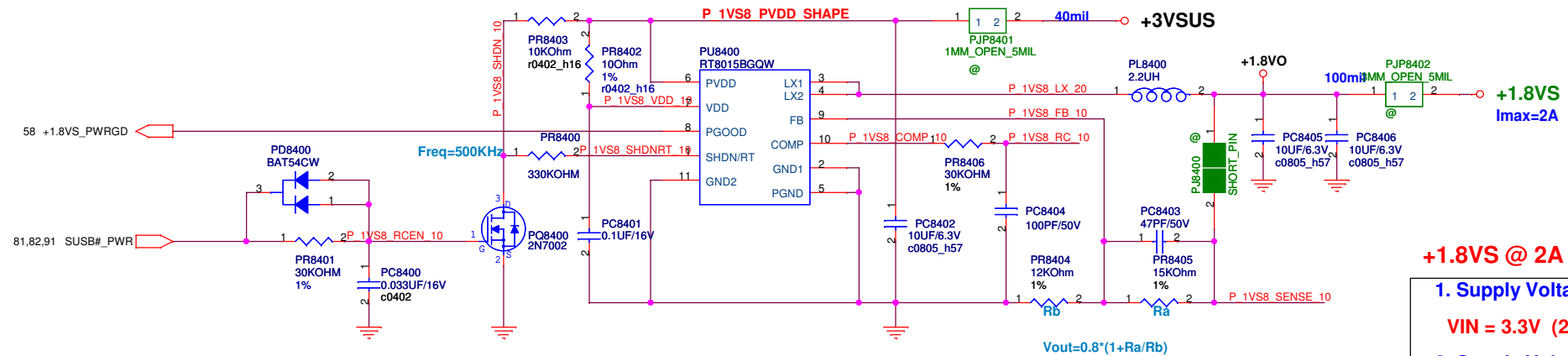
U35JC

2.00

Date: Friday, April 09, 2010

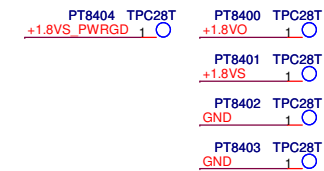
Sheet 63 of 99

+1.8VS POWER SUPPLY



+1.8VS @ 2A

1. Supply Voltage:
 $V_{IN} = 3.3V$ (2.6V ~ 5.5V)
2. Supply Voltage:
 $V_{OUT} = 1.8V / 2A$
3. Current Limit:
 $I_{limit} = 3.2A$
4. Continue Current:
 $I_{cont} = 1A$
5. Feedback Voltage:
 $V_{FB} = 0.8V$
6. Switching Frequency:
 $R_{rt} = 330\text{ Kohm}$
 $F_{sw} = 1000\text{KHz}$



<Variant Name>



Title : *POWER_I/O_+1.8VS*

ASUSTeK COMPUTER INC. NB

Engineer: **Morris/Sting**

Size B	Project Name
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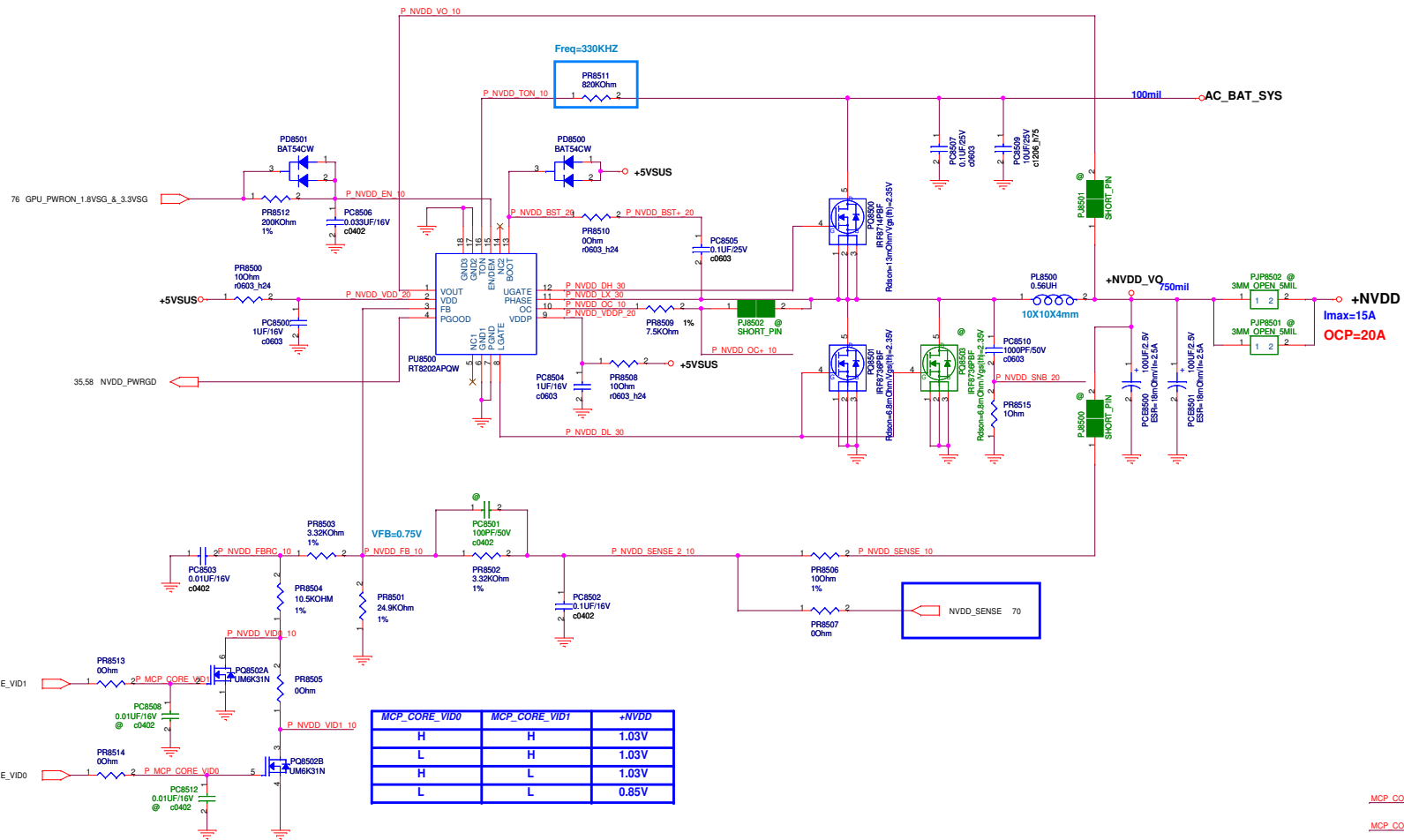
U35JC

Rev	
2.00	

Date: Friday, April 09, 2010

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GPU NVDD POWER SUPPLY



Power stage

NVDD:

1. I/P Current:
 $I_{in} = V_o \cdot I_o / (0.75 \cdot V_{in}) = 2.11A$
2. Ripple Current:
 $I_{rip} = 6.4A$
3. Ripple Voltage:
 $ESR / 2 = 7.5m\Omega$
 $V = 48mV$
4. Inductor Spec:
 $I_{sat} = 26A$
 $I_{dc} = 17.5A$
 $DCR = 4.2m\Omega$
5. MOSFET Spec:
 H-side MOSFET: RJK0355DPA
- | | |
|----------------------------|----------------------------------|
| $R_{ds}(ON) = 16.5m\Omega$ | $(V_{gs} = 4.5 \text{ V})$ |
| $I_{cont} = 30A$ | $(T = 25 \text{ } ^\circ C)$ |
| $I_{peak} = 120A$ | $(\text{Pause} = 10 \text{ us})$ |
- L-side MOSFET: RJK0353DPA
- | | |
|---------------------------|----------------------------------|
| $R_{ds}(ON) = 7.6m\Omega$ | $(V_{gs} = 4.5 \text{ V})$ |
| $I_{cont} = 35A$ | $(T = 25 \text{ } ^\circ C)$ |
| $I_{peak} = 140A$ | $(\text{Pause} = 10 \text{ us})$ |

Controller

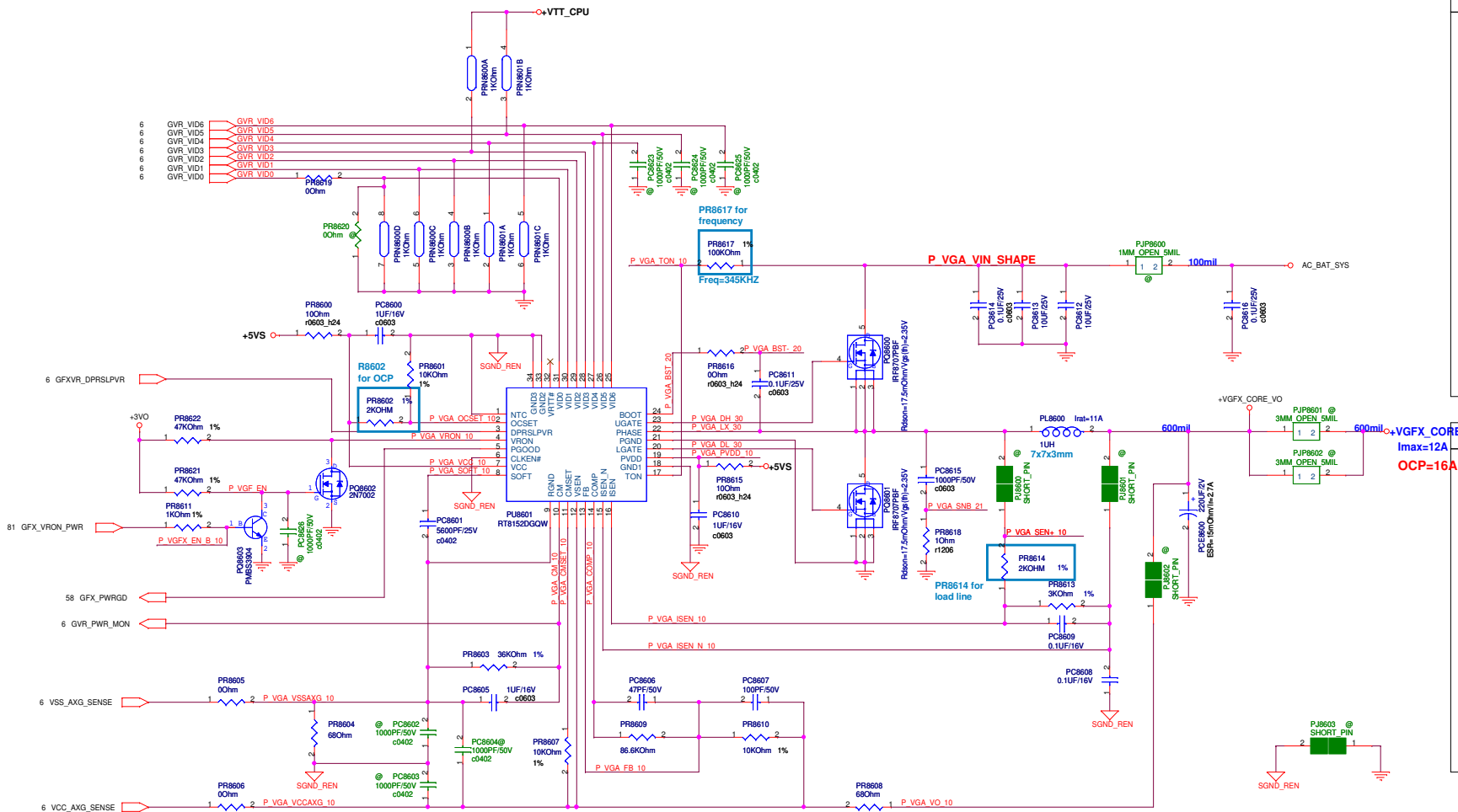
NVDD:

1. **Voltage & Current:**
+NVDD: 0.95V / 15A
2. **Frequency:**
F=300KHZ
3. **OCp:**
Set R8504=7.5 Kohm
Iocp=Rocp*20uA/Rds(on)
Iocp=20A
4. **Soft start time:**
The Soft Start duration is 1.35ms
5. **Inrush Current:**
C total = 440 uF
I inrush=C*Vout/SS_time
I inrush= 0.310 A

MCP_CORE_VID0	MCP_CORE_VID1	+NVDD
H	H	1.03V
L	H	1.03V
H	L	1.03V
L	L	0.85V

MCP_CORE_VID0	PT8511	TPC28T	1	0	PT8503	TPC28T	1	0
					..NVDD			
MCP_CORE_VID1	PT8513	TPC28T	1	0	PT8504	TPC28T	1	0
					..NVDD			
GPU_PWON 1.8VSG & 3.3VSG	PT8510	TPC28T	1	0	PT8500	TPC28T	1	0
					..NVDD			
NVDD_PWRGD	PT8509	TPC28T	1	0	PT8507	TPC28T	1	0
					..NVDD_VO			
NVDD_SENSE	PT8512	TPC28T	1	0	PT8508	TPC28T	1	0
					..NVDD_VO			
					PT8501	TPC28T	1	0
					..GND			
					PT8502	TPC28T	1	0
					..GND			
					PT8505	TPC28T	1	0
					..GND			
					PT8506	TPC28T	1	0
					..GND			

RENDER CORE POWER SUPPLY




Power stage
+VGFX: 1. I/P Current: $I_{in} = V_o \cdot I_o / (0.75 \cdot V_{in}) = 2.22A$ 2. Ripple Current: $I_{rip} = 7.28A$ 3. Ripple Voltage: $ESR/2 = 7.5mohm$ $V = 54.6mV$ 4. Inductor Spec: $I_{sat} = 26A$ $I_{dc} = 17.5A$ $DCR = 4.2mohm$ 5. MOSFET Spec: H-side MOSFET: RJK0355DPA $R_{ds(ON)} = 16.5mohm$ ($V_{gs} = 4.5V$) $I_{cont} = 30A$ ($T = 25^\circ C$) $I_{peak} = 120A$ (Pause = 10 us) L-side MOSFET: RJK0353DPA $R_{ds(ON)} = 7.6mohm$ ($V_{gs} = 4.5V$) $I_{cont} = 35A$ ($T = 25^\circ C$) $I_{peak} = 140A$ (Pause = 10 us)

Controller
+VGFX: 1. Voltage & Current: +VGFX: 1V / 15A 2. Frequency: $T_{on} = 241ns$ $R_{ton} = 150kohm$ $F_{sw} = 277KHz$ 3. OCP: $V_{ocset} = V_{CC} \cdot R_{8612} / (R_{8602} + R_{8612}) = 3.844V$ $I_{max} = V_{ocset} / (40 \cdot DCR) = 21A$ 4. Soft start time: The Soft Start duration is 0.75ms ($C_{ss} = 10nF$, $SOFT = 1.5V$) 5. Inrush Current: $C_{total} = 440uF$ $I_{inrush} = C \cdot V_{out} / SS_time$ $I_{inrush} = 0.587A$ 6. Load Line: DROOP = 7mohm

PT8623 TPC28T	PT8603 TPC28T	
VSS_AXG_SENSE_1	+VGFX_CORE_1	
PT8625 TPC28T	PT8604 TPC28T	
VCC_AXG_SENSE_1	+VGFX_CORE_1	
PT8621 TPC28T	PT8600 TPC28T	
GFX_PWRGD_1	+VGFX_CORE_1	
PT8626 TPC28T	PT8609 TPC28T	PT8610 TPC28T
GVR_PWR_MON_1	+VGFX_CORE_Vp	GVR_VID0_1
PT8619 TPC28T	PT8602 TPC28T	PT8611 TPC28T
P_VGF_EN_1	+VGFX_CORE_Vp	GVR_VID1_1
PT8617 TPC28T	PT8601 TPC28T	PT8612 TPC28T
P_VGF_EN_B_1p	+VGFX_CORE_Vp	GVR_VID2_1
PT8620 TPC28T	PT8606 TPC28T	PT8613 TPC28T
GFX_VRON_PWR_1	GND	GVR_VID3_1
PT8622 TPC28T	PT8605 TPC28T	PT8614 TPC28T
GFXVR_DPRSLPVR_1	GND	GVR_VID4_1
	PT8607 TPC28T	PT8615 TPC28T
	GND	GVR_VID5_1
	PT8608 TPC28T	PT8616 TPC28T
	GND	GVR_VID6_1

	5	4	3	2	1
D					
C					
B					
A					
	5	4	3	2	1

<Variant Name>



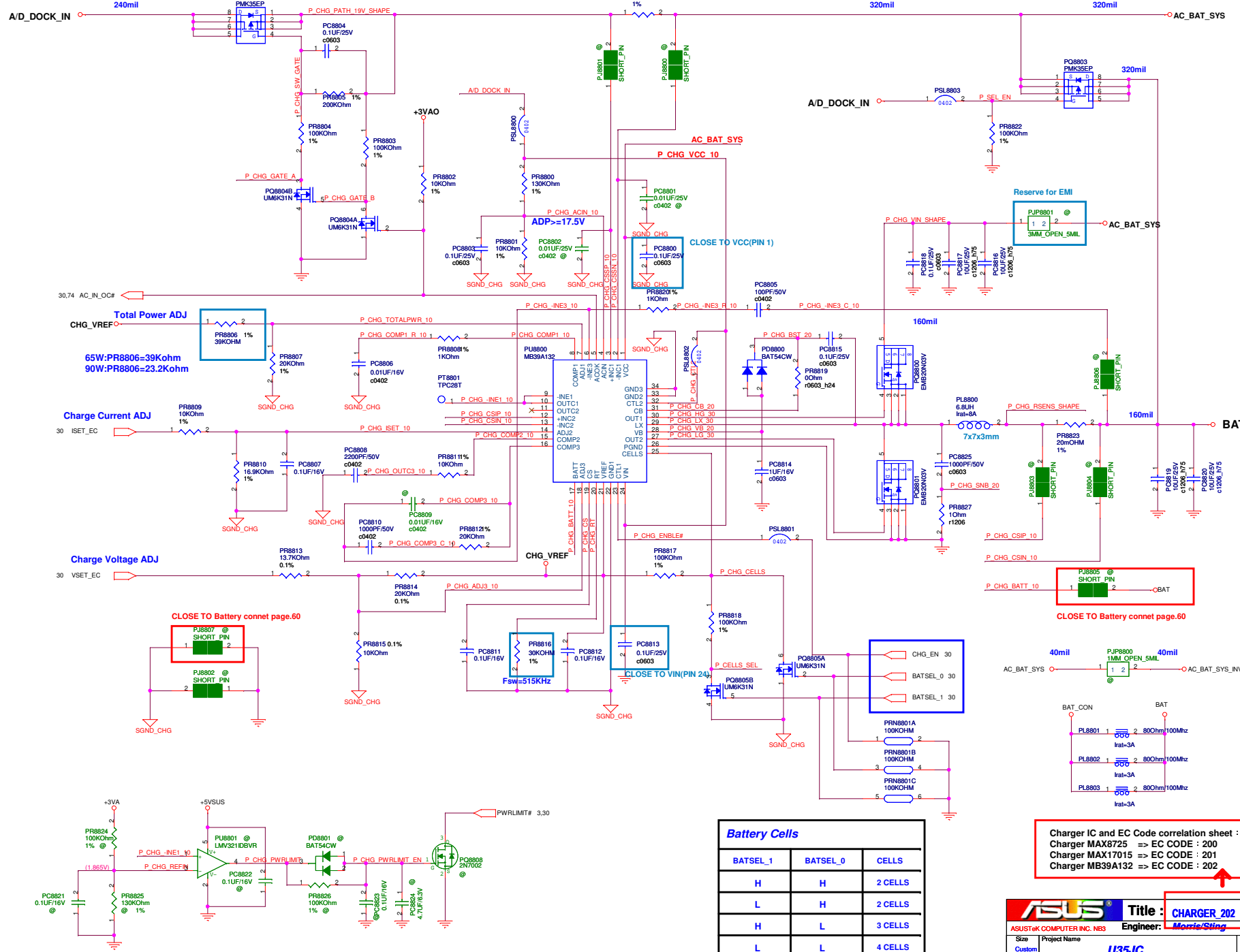
Title :

<OrgName>

Engineer:

Size	Project Name	Rev
Custom		1.1

Date: Friday, April 09, 2010Sheet 87 of 99




Battery Cells

BATSEL_1	BATSEL_0	CELLS
H	H	2 CELLS
L	H	2 CELLS
H	L	3 CELLS
L	L	4 CELLS

5	4	3	2	1
D				D
C				C
B				B
A				A
5	4	3	2	1

<Variant Name>



Title :

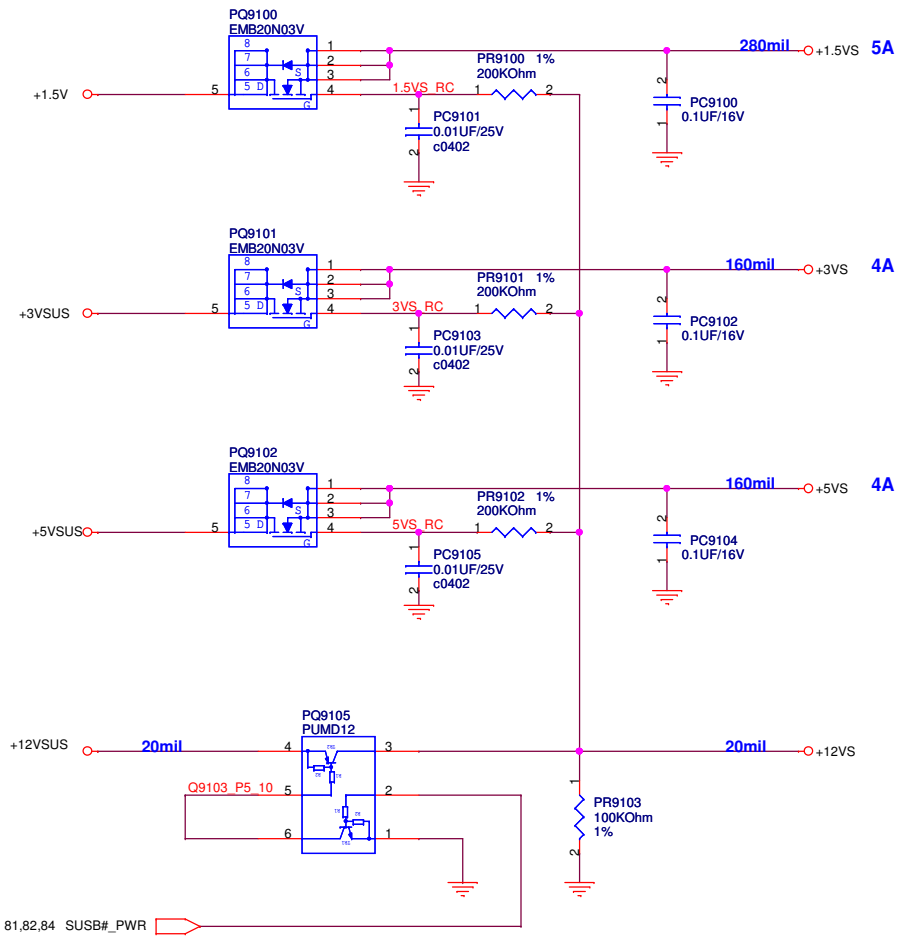
ASUSTeK COMPUTER INC. NB

Engineer:

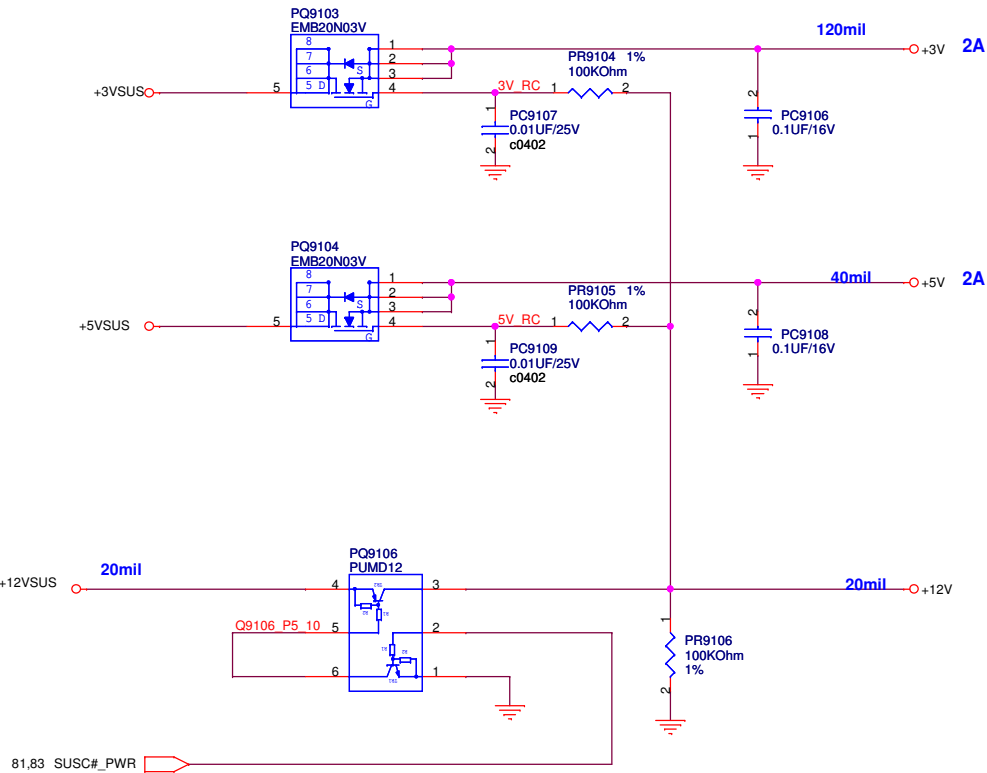
Size	Project Name	Rev
Custom		1.1

Date: Friday, April 09, 2010Sheet 90 of 99

SUSB#_PWR POWER



SUSC#_PWR POWER



PT9100	TPC28T	PT9104	TPC28T
+1.5VS	1	+3V	1
PT9101	TPC28T	PT9105	TPC28T
+3VS	1	+5V	1
PT9102	TPC28T	PT9106	TPC28T
+5VS	1	+12V	1
PT9103	TPC28T		
+12VS	1		

<Variant Name>

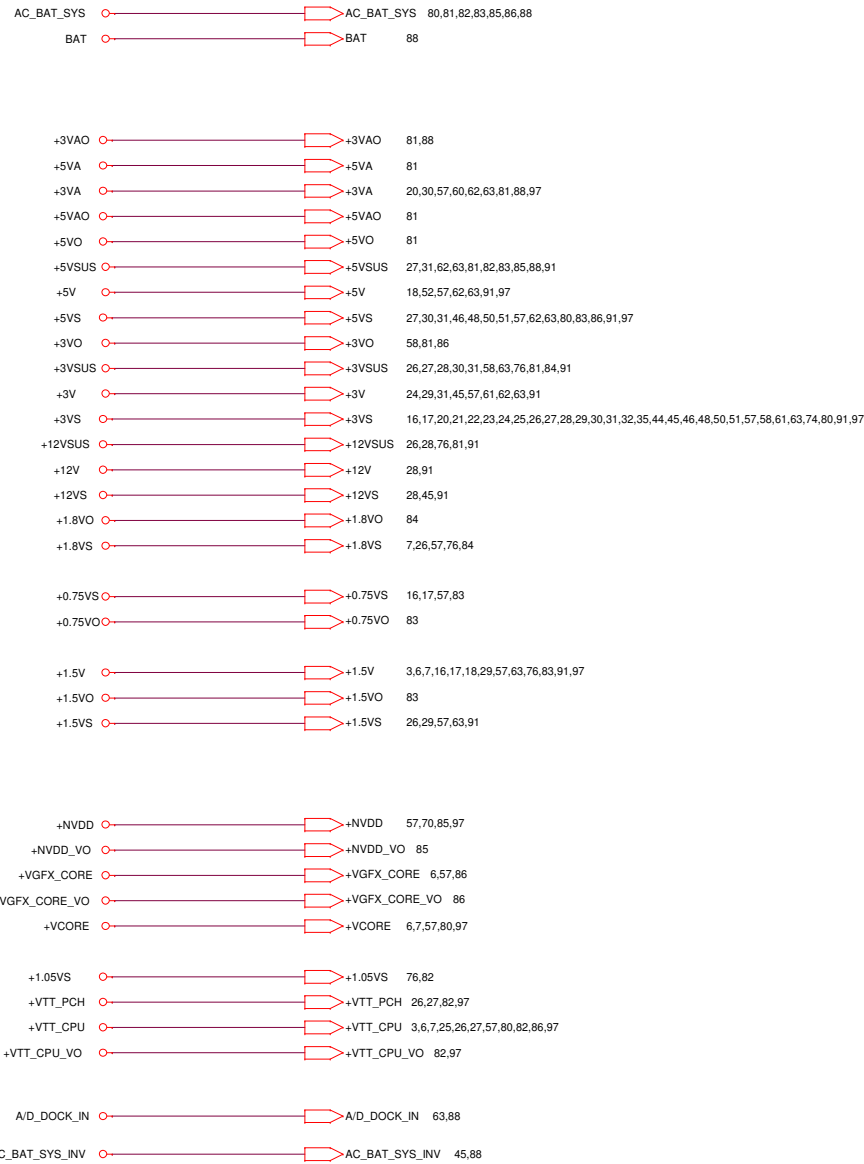
Title :POWER_LOAD SWITCH

ASUSTeK COMPUTER INC. NB Engineer: Morris/Sting

Size	Project Name	Rev
B	U35JC	2.00

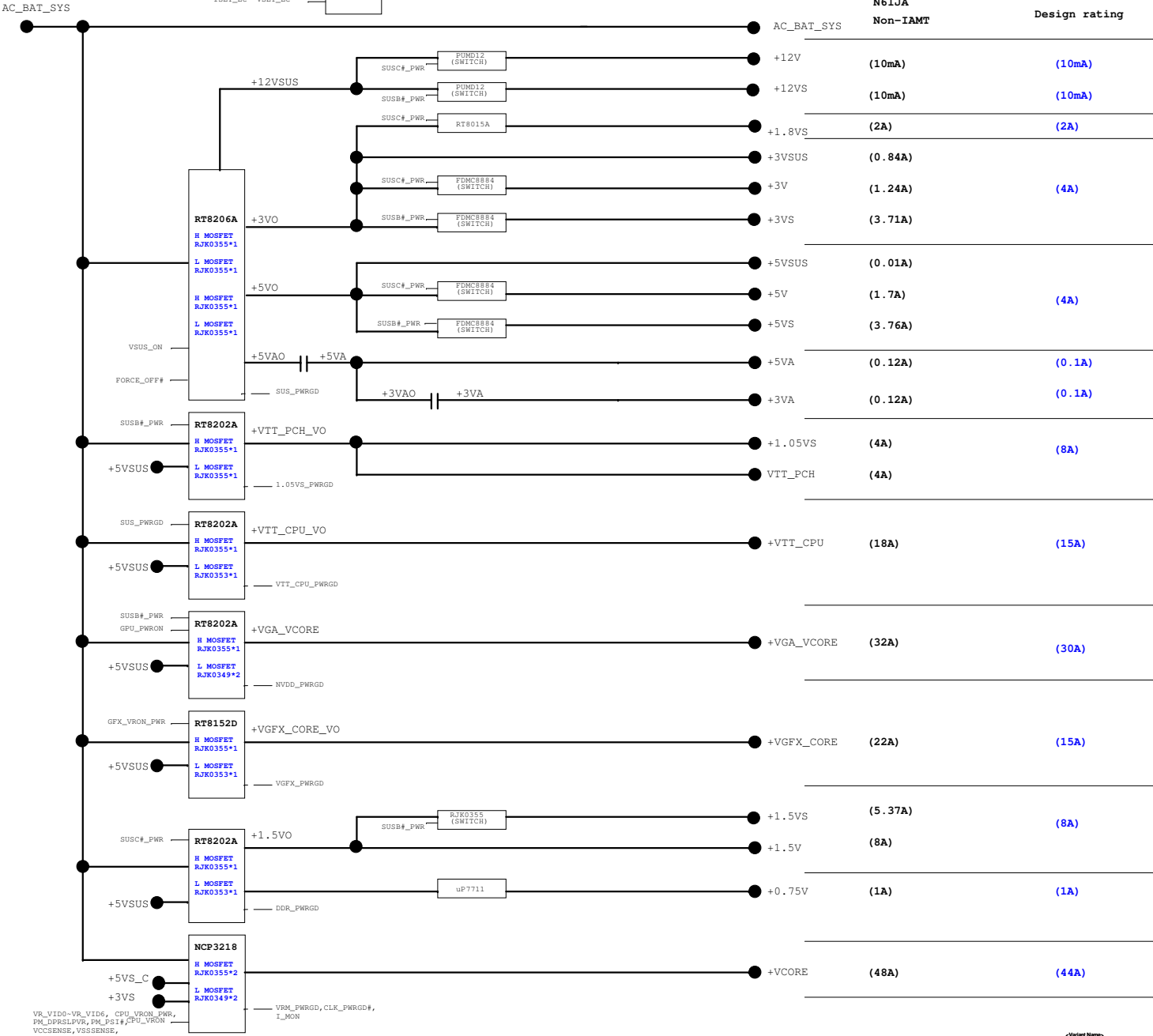
Date: Friday, April 09, 2010Sheet 91 of 99

Total count: 27 pcs



A/D_DOCK_IN

AC_BAT_SYS



N61JA
Non-IAMT
Design rating

(10mA) (10mA)

(10mA) (10mA)

(2A) (2A)

(0.84A)

(1.24A) (4A)

(3.71A)

(0.01A)

(1.7A) (4A)

(3.76A)

(0.12A) (0.1A)

(0.12A) (0.1A)

(4A) (8A)

(4A)

(18A) (15A)

(32A) (30A)

(22A) (15A)

(5.37A) (8A)

(8A)


(1A) (1A)

(48A) (44A)

Rev	Date	Description
1.00	01/08 '2010	First Release!
1.10	01/20 '2010	01. Swap Debug Connect, page 44 02. Modify circuit for AZWAVE/INTEL WiFi minicard, page 61 03. Mount EDID resistor fro MODS, R3532, R3533, R3590, R3591, page 35 04. Check Strap[0,1,2] setting for MP GPU, page 72
	01/22 '2010	05. Remove LVDS_GPU_SW/SW#, remove R3564, R3567, R3571, R3596, Q3552, page 35 06. Change CPU_DV0/CPU_DV1 to GPJ4/GPJ5, page30 07. Change VCCP_DV0/VCCP_DV1 to GPF2/GPF3, page30 08. Change MARATHON# to GPE7, page30
	01/27 '2010	09. Change LVDS CONN, page45 10. Check thermal sensor on PR, page50 11. XTAL 14.318MHz C2913, C2914 to 18PF, page29 12. Refer K72F to modify ICS9LVS3162B circuit, page 29 13. XTAL 27MHz C7308, C7309 to 27PF, page73 14.Change CLK_OC to Clock_select_uc, page 30 15.Change EC GPG2/GPG6 from CLK_STRAP[0,1] to T3019/T3020, paage 30 16.Change EC GPE5 from CLK_OC to T3021, paage 30

[M61JA] R1.0 => R1.1

- 1. Follow E.E RC delay
 - +5v R9107 100K change to 68K
 - +3v R9106 200K change to 121K
 - +1.5v R8306 49.9K change to 68K
 - +5VS R9104 200K change to 68K
 - +3VS R9103 200K change to 121K
 - +1.8VS R8401 33.2K change to 121K
 - +1.5VS R9102 470K change to 390K
 - +1.05VS R8252 39K change to 200K
 - +0.75VS R8312 0 change to 2.49K C8310 0.1U change to 2.2U
- 2.VR_VID0~2 pull high 1K VR_VID6 pull low 1K.
- 3.U8401 RT8015A change to RT8015B
- 4.Reserve GVR_VID0~VID6 pull high and low resistor R8627~R8633
- 5.Reserve R8517~R5720 pull high & pull low risistor for MCP_CORE_VID
- 6.page86 component option change to ARD (CFD no stuff)
- 7.R8004 option change to CFD & R8049 change to ARD(For IMON)
- 8.Change RN8801A RN8801B(layout request)
- 9.R8517 R8519 change to stuff
- 10.R8406 13K change to 12K
- 11.CE8005 no stuff , CE8007 stuff
- 12.C8403 C8406 size 0603 change to 0805
- 13.R8213 R8305 ohm change to 2.2 ohm
- 14.R8621~R8633 stuff 1K ohm
- 15.R8512 change form 200K to 33K ohm
- 16.VTT_PCH component option change to CFD
- 17.Delete U8502 & GPU_PWRON signal change to GPU_PWRON_1.8VSG_&_3.3VSG
- 18.L8601 1uH => 0.56uH , C8608 0.01uF/50 => 0.01uF/16V , R8621 43K => 36K , C8617 =>0.1uF/16V 1uF/10V , C8607 68pF/50V => 33pF/50V , R8625 10K => 18.7K , R8613 3.6K => 4.02K
- 19.R8057 change form 10K to 2.05K
- 20.Add Q8007 & Q8008 form thermal issue



Title : System History

ASUSTeK COMPUTER INC. NBEngineer:

Size

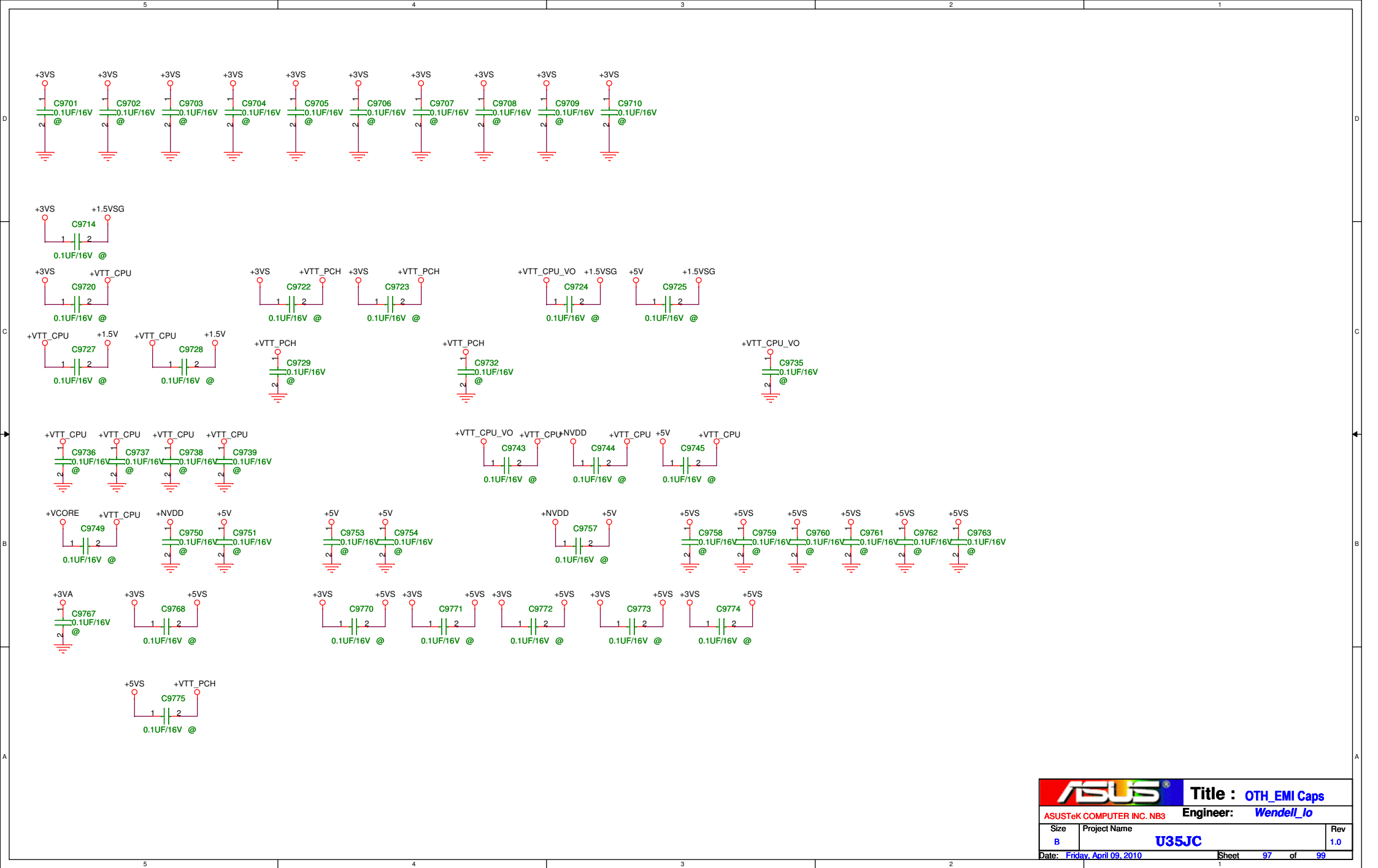
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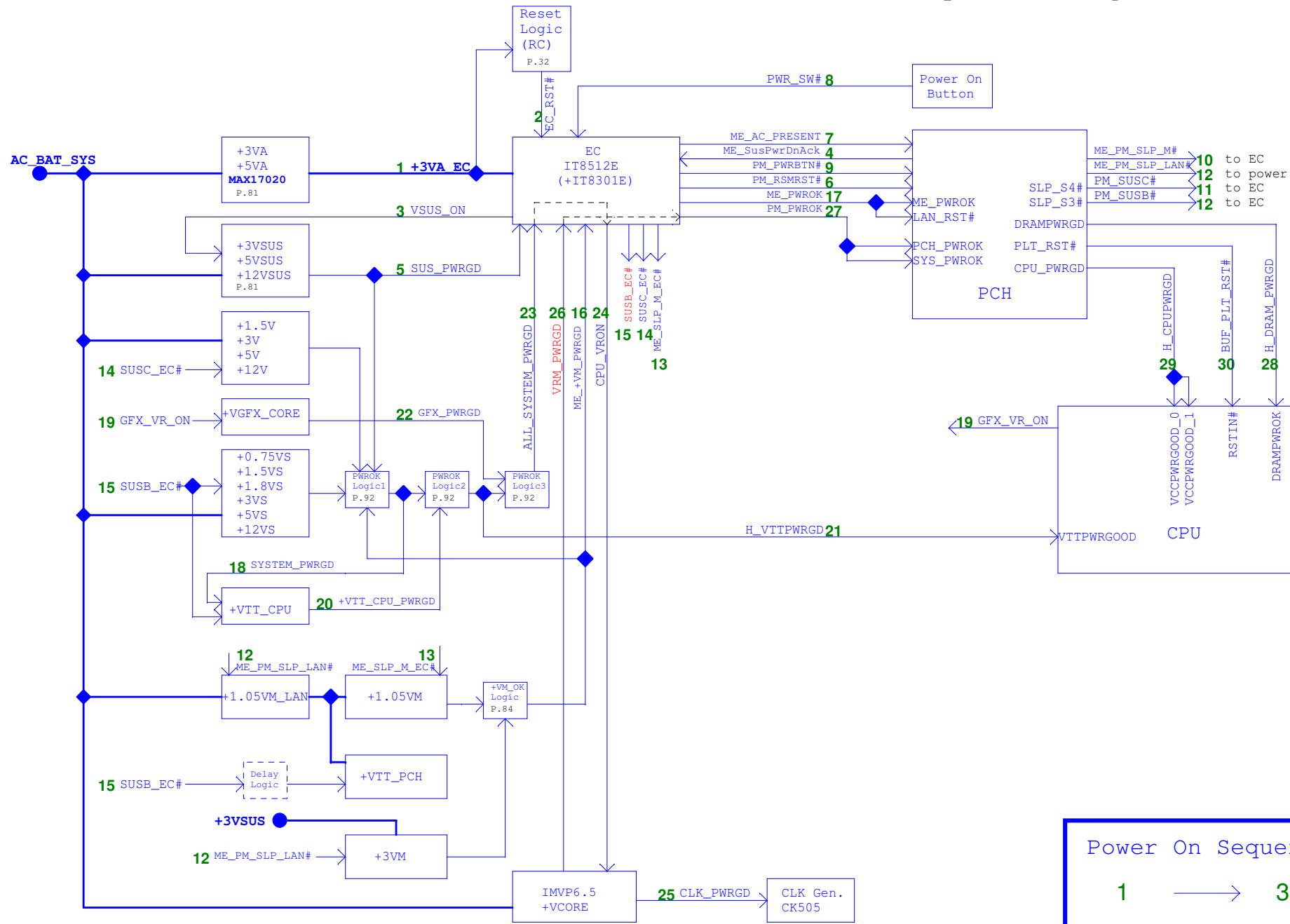
Project Name

U35JC

Date: Friday, April 09, 2010

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Power On Sequence

1 → 30

AC-IN Mode

M52J Power-On Sequence
Timing Diagram Rev.0.31

